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Technical Reference: Pinouts for Serial Interfaces

This Technical Reference describes the pinouts specified and used for the more common serial data-communication interfaces. Given its space limitations and the speed with which new interfaces and connectors render older ones obsolete, this document is not intended to be comprehensive or exhaustive. We do hope, however, that you will find it useful as you study, shop for, build, or troubleshoot devices and cables.

Notes: For all of the interfaces described here, when any signal's function/direction is listed as "Data, to DCE," DCEs receive data and DTEs transmit data on that lead; when the function/direction is listed as "Data, from DCE," DCEs transmit data and DTEs receive data on that lead. All connectors are shown in front view (wires exit from the rear). The "pins" on male connectors are typically metal prongs, while those on female connectors are typically metal-lined sockets.

To compare interface pinouts, match their V.24 circuit-reference numbers, or see the side-by-side chart on page 7.

1. EIA-232-D (RS-232-D), ITU-TSS (CCITT) V.24/V.28, ISO 2110

A. Original standard pinout on DB25 connectors:



Pin	Signal/Circuit Name	Abbreviation*	RS-232 Circuit Ref.	V.24 Circ. Ref.	Signal Function/Direction
1	Shield—"Protective Ground," "Frame Ground," "Chassis Ground"	SHD ("PGND," etc.)	AA	101	Ground
2	Transmitted Data	TD ("TXD")	BA	103	Data, to DCE
3	Received Data	RD ("RXD")	BB	104	Data, from DCE
4	Request to Send	RTS	CA	105	Control, to DCE
5	Clear to Send	CTS	CB	106	Control, from DCE
6	DCE Ready—"Data Set Ready"	DCR ("DSR")	CC	107	Control, from DCE
7	Signal Ground—"Common Return"	SGND	AB	102	Ground
8	Received Line Signal Detector—"Carrier Detect," "Data Carrier Detect"	RLSD ("CD," "DCD")	CF	109	Control, from DCE
(9 = +12 VDC reserved for testing, 10 = -12 VDC reserved for testing, 11 = Unassigned)					
12	Either Secondary Received Line Signal Detector—"Secondary Carrier Detect," "Secondary Data Carrier Detect"— or Data Signal Rate Selector (DCE Source)	SRLSD ("SCD," "SDCD") DSRSC	SCF CI	122 112	Control, from DCE Control, from DCE
13	Secondary Clear to Send	SCTS	SCB	121	Control, from DCE
14	Secondary Transmit Data	STD ("STXD")	SBA	118	Data, to DCE
15	Transmitter Signal Element Timing (DCE Source)—"Transmit Clock"	TSETC ("TC," "TXC")	DB	114	Timing, from DCE
16	Secondary Receive Data	SRD ("SRXD")	SBB	119	Data, from DCE
17	Receiver Signal Element Timing (DCE Source)—"Receive Clock"	RSETC ("RC," "RXC")	DD	115	Timing, from DCE
18	Local Loopback	LL	LL	141	Control, to DCE
19	Secondary Request to Send	SRTS	SCA	120	Control, to DCE
20	DTE Ready—"Data Terminal Ready"	DTR	CD	108.2	Control, to DCE

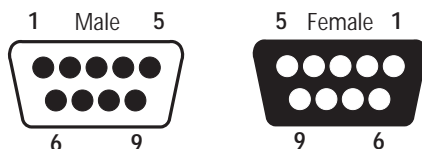
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*These are de-facto standard abbreviations; the official EIA-232-D standard does not specify abbreviations for the signal names.

Pin	Signal/Circuit Name	Abbreviation*	RS-232 Circuit Ref.	V.24 Circ. Ref.	Signal Function/Direction
21	Either Remote Loopback or Signal Quality Detector	RL SQD	RL CG	140 110	Control, to DCE Control, from DCE
22	Ring Indicator	RI	CE	125	Control, from DCE
23	Either Data Signal Rate Selector (DTE Source) or Data Signal Rate Selector (DCE Source)	DSRST DSRSC	CH CI	111 112	Control, to DCE Control, from DCE
24	Transmitter Signal Element Timing (DTE Source)—“External Clock”	TSETT (“EXTC”)	DA	113	Timing, to DCE
25	Test Mode—“Test Indicator”	TM (“TI”)	TM	142	Control, from DCE

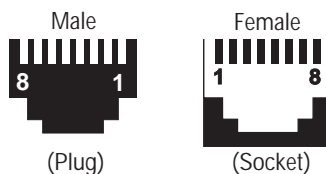
Note that many applications use only a subset of this pinout: **16 pins**—1 through 8, 15, 17, and 20 through 25—for synchronous communication with secondary control and testing; **12 pins**—1 through 8, 15, 17, 20, and 22—for ordinary sync applications; **7 pins**—2 through 4, 6 through 8, and 20—for asynchronous communication with flow control; or the **4 pins** 2, 3, 7, and 20 for bare-bones async applications that use software flow control.

B. EIA/TIA-574 pinout (used for IBM® AT® and compatible computers) on DB9 (DE9) connectors:



Pin	Signal/Circuit Name	Abbreviation*	RS-232 Circuit Ref.	V.24 Circ. Ref.	Signal Function/Direction
1	Received Line Signal Detector—“Carrier Detect,” “Data Carrier Detect”	RLSD (“CD,” “DCD”)	CF	109	Control, from DCE
2	Received Data	RD (“RXD”)	BB	104	Data, from DCE
3	Transmitted Data	TD (“TXD”)	BA	103	Data, to DCE
4	DTE Ready—“Data Terminal Ready”	DTR	CD	108.2	Control, to DCE
5	Signal Ground—“Common Return”	SGND	AB	102	Ground
6	DCE Ready—“Data Set Ready”	DCR (“DSR”)	CC	107	Control, from DCE
7	Request to Send	RTS	CA	105	Control, to DCE
8	Clear to Send	CTS	CB	106	Control, from DCE
9	Ring Indicator	RI	CE	125	Control, from DCE

C. EIA/TIA-561 pinout (also referred to as ANSI/EIA-232-D) on RJ-45 connectors (unfortunately, most manufacturers use proprietary pinouts instead):



Pin	Signal/Circuit Name	Abbreviation*	RS-232 Circuit Ref.	V.24 Circ. Ref.	Signal Function/Direction
1	Either DCE Ready—“Data Set Ready”—or Ring Indicator	DCR (“DSR”) RI	CC CE	107 125	Control, from DCE Control, from DCE
2	Received Line Signal Detector—“Carrier Detect,” “Data Carrier Detect”	RLSD (“CD,” “DCD”)	CF	109	Control, from DCE
3	DTE Ready—“Data Terminal Ready”	DTR	CD	108.2	Control, to DCE
4	Signal Ground—“Common Return”	SGND	AB	102	Ground
5	Received Data	RD (“RXD”)	BB	104	Data, from DCE
6	Transmitted Data	TD (“TXD”)	BA	103	Data, to DCE
7	Clear to Send	CTS	CB	106	Control, from DCE
8	Request to Send	RTS	CA	105	Control, to DCE

*These are de-facto standard abbreviations; the official EIA-232-D standard does not specify abbreviations for the signal names.

2. EIA-422-A (RS-422-A), ITU-TSS (CCITT) V.11/X.27; also ITU-TSS G.703, EIA-485 (RS-485)

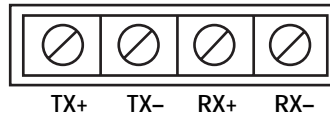
EIA-422-A and its ITU-TSS counterpart V.11/X.27 are electrical standards for balanced (matched-pair) circuits only; NO PHYSICAL CONNECTOR IS SPECIFIED. When manufacturers want to implement them on the fewest possible contacts, they use a four-position terminal block (for Transmit [TX] + and – and Receive [RX] + and –), roughly as shown below. (Sometimes a fifth terminal is added for a shield or protective ground contact.) Though a screw-down terminal block is shown, most manufacturers today use “snap”- or “crimp”-type terminals to comply with electrical safety standards. These standards are also frequently implemented on DB37 (DC37) connectors pinned as EIA-449 (see **Section 5**) or on DB25 connectors pinned as EIA-530 (see **Section 6**).

All of the above is also true of ITU-TSS G.703, but G.703 also specifies sophisticated coding schemes and other protocols. Also, some G.703 devices can autosense polarity, so “+” and “–” are sometimes not labeled on the block.

EIA-485 is very similar to EIA-422-A, except that its signal-generator and -receiver circuitry can handle three electrical states instead of two. This makes it ideal for multipoint applications, unlike the other interfaces listed here.

Aside from one being balanced and the other unbalanced, EIA-422-A and EIA-423-A are identical.

Typical basic pinout on a 4-position terminal block:

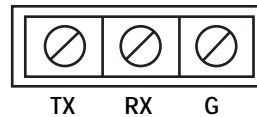


3. EIA-423-A (RS-423-A), ITU-TSS (CCITT) V.10/X.26

EIA-423-A and its ITU-TSS counterpart V.10/X.26 are electrical standards for unbalanced (unmatched, ground-referenced) circuits only; NO PHYSICAL CONNECTOR IS SPECIFIED. When manufacturers want to implement them on the fewest possible contacts, they use a three-position terminal block (for Transmit [TX], Receive [RX], and Ground [G]), roughly as shown below. Though a screw-down terminal block is shown, most manufacturers today use “snap”- or “crimp”-type terminals to comply with electrical safety standards. These standards are also frequently implemented on DB37 and DB9 connectors pinned as EIA-449 (see **Section 5**) or on DB25 connectors pinned as EIA-530 (see **Section 6**).

Aside from one being balanced and the other unbalanced, EIA-422-A and EIA-423-A are identical.

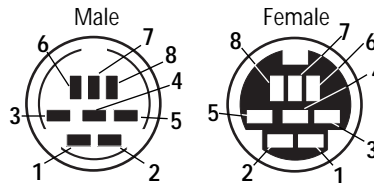
Typical basic pinout on a 3-position terminal block:



4. Apple® Macintosh® Serial

In Apple Macintosh serial (modem and printer) ports and in the serial ports on some Apple printers and modems, the data signals are balanced EIA-422-A signals, while the handshaking signals are unbalanced EIA-423-A signals.

Pinout on **8-pin mini-DIN** (“**mini-DIN-8**”) connectors:



Pin	Signal/Circuit Name	Abbrev.	Signal Function/Direction	Pin	Signal/Circuit Name	Abbrev.	Signal Function/Direction
1	Handshake Output (DTR)	HSKo, +12V	Control, to DCE	5	Received Data (Minus)	RXD–	Data, from DCE
2	Handshake Input (DSR)	HSKG	Control, from DCE	6	Transmitted Data (Plus)	TXD+	Data, to DCE
3	Transmitted Data (Minus)	TXD–	Data, to DCE	7	Unassigned		
4	Signal Ground	GND	Ground	8	Received Data (Plus)	RXD+	Data, from DCE

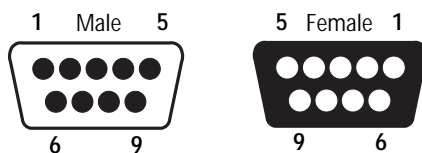
5. EIA-449 (RS-449), ISO 4902

A. Primary channel pinout on DB37 (DC37) connectors:



Pin	Signal/Circuit Name*	Mnem.	V.24 Circ. Ref.	Signal Function/ Direction	Pin	Signal/Circuit Name*	Mnem.	V.24 Circ. Ref.	Signal Function/ Direction
1	Shield	AA	101	Ground	20	Receive Common	RC	102b	Ground
2	Signal Rate Indicator	SI	112	Control, from DCE	21	Unassigned			
3	Unassigned				22	Send Data B	SD B	103	Data, to DCE
4	Send Data A	SD A	103	Data, to DCE	23	Send Timing B	ST B	114	Timing, from DCE
5	Send Timing A	ST A	114	Timing, from DCE	24	Receive Data B	RD B	104	Data, from DCE
6	Receive Data A	RD A	104	Data, from DCE	25	Request to Send B	RS B	105	Control, to DCE
7	Request to Send A	RS A	105	Control, to DCE	26	Receive Timing B	RT B	115	Timing, from DCE
8	Receive Timing A	RT A	115	Timing, from DCE	27	Clear to Send B	CS B	106	Control, from DCE
9	Clear to Send A	CS A	106	Control, from DCE	28	Terminal In Service	IS	[N/A]	Control, to DCE
10	Local Loopback	LL	141	Control, to DCE	29	Data Mode B	DM B	107	Control, from DCE
11	Data Mode A	DM A	107	Control, from DCE	30	Terminal Ready B	TR B	108.2	Control, to DCE
12	Terminal Ready A	TR A	108.2	Control, to DCE	31	Receiver Ready B	RR A	109	Control, from DCE
13	Receiver Ready A	RR A	109	Control, from DCE	32	Select Standby	SS	116	Control, to DCE
14	Remote Loopback	RL	140	Control, to DCE	33	Signal Quality	SQ	110	Control, from DCE
15	Incoming Call	IC	125	Control, from DCE	34	New Signal	NS	[N/A]	Control, to DCE
16	Select Frequency	SF	126	Control, from DCE	35	Terminal Timing B	TT B	113	Timing, to DCE
17	Terminal Timing A	TT A	113	Timing, to DCE	36	Standby Indicator	SB	117	Control, from DCE
18	Test Mode	TM	142	Control, from DCE	37	Send Common	SC	102a	Ground
19	Signal Ground	SG	102	Ground					

B. Secondary (auxiliary) channel pinout on DB9 (DE9) connectors:

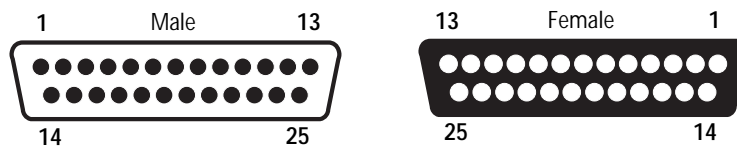


Pin	Signal/Circuit Name*	Mnem.	V.24 Circ. Ref.	Signal Function/ Direction	Pin	Signal/Circuit Name*	Mnem.	V.24 Circ. Ref.	Signal Function/ Direction
1	Shield	AA	101	Ground	6	Receive Common	RC	102b	Ground
2	Secondary Rcvr. Ready	SRR	122	Control, from DCE	7	Secondary Rq. to Send	SRS	120	Control, to DCE
3	Secondary Send Data	SSD	118	Data, to DCE	8	Secondary Clr. to Send	SCS	121	Control, from DCE
4	Secondary Rcv. Data	SRD	119	Data, from DCE	9	Send Common	SC	102a	Ground
5	Signal Ground	SG	102	Ground					

*Signals whose names end with A and B are balanced (EIA-422-A compatible) and are classified as "Category I"; the A signals are positive with respect to the B signals during "space" (logical 0) conditions, and negative with respect to the B signals during "mark" (logical 1) conditions. All non-ground signals whose names don't end with A or B are unbalanced (EIA-423-A compatible) and are classified as "Category II."

6. EIA-530 (RS-530)

Pinout on DB25 connectors:



Pin	Signal/Circuit Name ^{1, 2}	Abbrev. ^{2, 3}	RS-530 Circuit Ref.	V.24 Circ. Ref.	Signal Function/ Direction
1	Shield	SHD	AA	101	Ground
2	Transmitted Data A	TD A	BA	103	Data, to DCE
3	Received Data A	RD A	BB	104	Data, from DCE
4	Request to Send A	RTS A	CA	105	Control, to DCE
5	Clear to Send A	CTS A	CB	106	Control, from DCE
6	DCE Ready A	DCR A	CC	107	Control, from DCE
7	Signal Ground	SGND	AB	102	Ground
8	Received Line Signal Detector A	RLSD A	CF	109	Control, from DCE
9	Receiver Signal Element Timing (DCE Source) B	RSETC B	DD	115	Timing, from DCE
10	Received Line Signal Detector B	RLSD B	CF	109	Control, from DCE
11	Transmitter Signal Element Timing (DTE Source) B	TSETT B	DA	113	Timing, to DCE
12	Transmitter Signal Element Timing (DCE Source) B	TSETC B	DB	114	Timing, from DCE
13	Clear to Send B	CTS B	CB	106	Control, from DCE
14	Transmitted Data B	TD B	BA	103	Data, to DCE
15	Transmitter Signal Element Timing (DCE Source) A	TSETC A	DB	114	Timing, from DCE
16	Received Data B	RD B	BB	104	Data, from DCE
17	Receiver Signal Element Timing (DCE Source) A	RSETC A	DD	115	Timing, from DCE
18	Local Loopback	LL	LL	141	Control, to DCE
19	Request to Send B	RTS B	CA	105	Control, to DCE
20	DTE Ready A	DTR A	CD	108.2	Control, to DCE
21	Remote Loopback	RL	RL	140	Control, to DCE
22	DCE Ready B	DCR B	CC	107	Control, from DCE
23	DTE Ready B	DTR B	CD	108.2	Control, to DCE
24	Transmitter Signal Element Timing (DTE Source) A	TSETT A	DA	113	Timing, to DCE
25	Test Mode	TM	TM	142	Control, from DCE

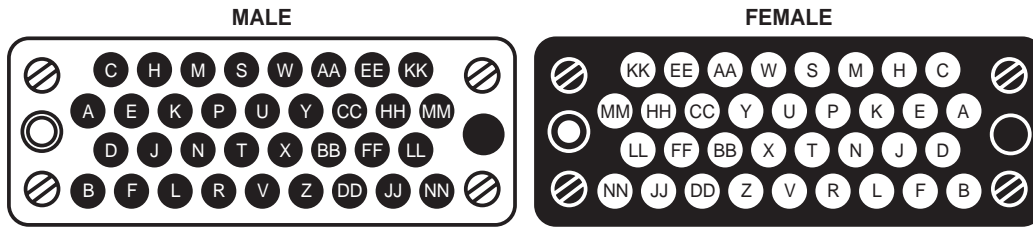
¹Signals whose names end with A and B are balanced (EIA-422-A compatible) and are classified as “Category I”; the A signals are positive with respect to the B signals during “space” (logical 0) conditions, and negative with respect to the B signals during “mark” (logical 1) conditions. The non-ground signals whose names don’t end with A or B—namely Local Loopback, Remote Loopback, and Test Mode—are unbalanced (EIA-423-A compatible) and are classified as “Category II.”

²The same alternative names and abbreviations that are sometimes used to describe some of the signals in EIA-232-D are also sometimes used to describe the analogous EIA-530 signals. See **Section 1**.

³These are de-facto standard abbreviations; the official EIA-530 standard does not specify abbreviations for the signal names.

7. ITU-TSS (CCITT) V.35

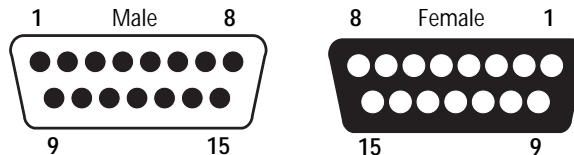
Pinout on M/34 (“34-pin M-block”) connectors:



Pin ¹	Signal/Circuit Name ^{2,3}	Abbr. ^{3,4}	V.24 Circ. Ref.	Signal Function/ Direction	Pin ¹	Signal/Circuit Name ^{2,3}	Abbr. ^{3,4}	V.24 Circ. Ref.	Signal Function/ Direction
A	Shield	SHD	101	Ground	P	Send Data A	TD A	103	Data, to DCE
B	Signal Ground	SGND	102	Ground	R	Receive Data A	RD A	104	Data, from DCE
C	Request to Send	RTS	105	Control, to DCE	S	Send Data B	TD B	103	Data, to DCE
D	Clear to Send	CTS	106	Control, from DCE	T	Receive Data B	RD B	104	Data, from DCE
E	Data Set Ready	DSR	107	Control, from DCE	U	Serial Clk. Tmit. Extnal. A ⁵	SCTE A	113	Timing, to DCE
F	Rcvd. Line Sgnl. Detector	RLSD	109	Control, from DCE	V	Serial Clock Receive A	SCR A	115	Timing, from DCE
H	Data Terminal Ready ⁵	DTR	108.2	Control, to DCE	W	Serial Clk. Tmit. Extnal. B ⁵	SCTE B	113	Timing, to DCE
J	Calling Indicator ⁶	CI	125	Control, from DCE	X	Serial Clock Receive B	SCR B	115	Timing, from DCE
L	Local Loopback ⁶	LL	141	Control, to DCE	Y	Serial Clock Transmit A	SCT A	114	Timing, from DCE
N	Remote Loopback ⁶	RL	140	Control, to DCE	AA	Serial Clock Transmit B	SCT B	114	Timing, from DCE
(K, M, Z, BB through FF, and MM are reserved for future int'l standardization. HH through LL are reserved for country-specific standards.)					NN	Test Mode ⁶	TM	142	Control, from DCE

8. ITU-TSS (CCITT) X.21, ISO 4903

High-speed, X.27-compatible pinout on DB15 (DA15) connectors:



Pin	Signal/Circuit Name ²	X.21 Circ. Ref.	V.24 Circ. Ref.	Signal Function/ Direction	Pin	Signal/Circuit Name ²	X.21 Circ. Ref.	V.24 Circ. Ref.	Signal Function/ Direction
1	Shield	SHD	101	Ground	9	Transmit B	T (B)	103	Data, to DCE
2	Transmit A	T (A)	103	Data, to DCE	10	Control B	C (B)	105	Control, to DCE
3	Control A	C (A)	105	Control, to DCE	11	Receive B	R (B)	104	Data, from DCE
4	Receive A	R (A)	104	Data, from DCE	12	Indication B	I (B)	109	Control, from DCE
5	Indication A	I (A)	109	Control, from DCE	13	Signal Element Timing B	S (B)	114	Timing, from DCE
6	Signal Element Timing A	S (A)	114	Timing, from DCE	14	Byte Timing B	B (B)	[N/A]	Timing, from DCE
7	Byte Timing A	B (A)	[N/A]	Timing, from DCE	15	Reserved for future international use			
8	Signal Ground	G	102	Ground					

¹V.35 pins designated with two capital letters (“AA,” “BB,” etc.) can be designated with single lowercase letters (“a,” “b,” etc.) instead.

²Signals whose names end with A and B are balanced; they are positive or negative with respect to each other depending on mark or space conditions (refer to note 1 on the previous page). All non-ground signals whose names don’t end with A or B are unbalanced.

³The same alternative names and abbreviations that are sometimes used to describe some of the signals in EIA-232-D are also sometimes used to describe the analogous V.35 signals. See **Section 1**.

⁴These are de-facto standard abbreviations; the official V.35 standard does not specify abbreviations for the signal names.

⁵These signals are officially optional but are almost always implemented—almost always on these pins.

⁶These signals are officially optional, but most manufacturers either don’t implement them or implement them on different pins.

