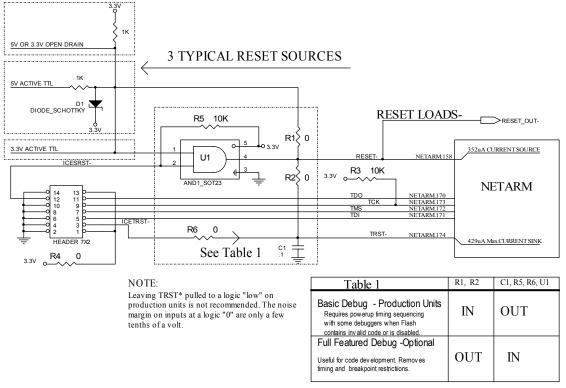
Some customers have run into problems gaining control of the NET+ARM processor after it has executed illegal instructions. This can happen if the flash ROM is corrupted, or is disconnected. Netsilicon has investigated this problem. Up to now we designed the JTAG interface on our development boards according to the *Basic nTRST Connection* described in ARM's <u>Application Note 31</u>, and have passed these recommendations onto our customers as well. This design ties NET+ARM TRST- and RESET- together. We have found that this design does not always allow a JTAG debugger ICE to gain control of the processor after it has executed illegal instructions. The nSRST and nTRST signals need to be kept separate. The nSRST signal should be connected to nRESET on the processor, and nTRST should be connected to nTRST on the processor. The schematic below shows the correct design. Customers should use this design in all new boards.



Both the Raven and Jeeni JTAG debug tools can be configured to reliably gain control of boards that use the design above.

## **Configure the Raven as follows:**

 Download and unzip this file: raven\_jtag\_fix.zip

from the NetSilicon, Inc FTP Site:

ftp://NetSupport:techsupport01@ftp.netsilicon.com/Private/Service Support/Raven Fix/

- 2. Move all 3 unzipped files into the \ghs\arm35 directory after Green Hills 3.5 is installed.
- 3. Use CPU type NETARM in Green Hills Multi.

## Configure the Jeeni ICE as follows:

- 1. Make sure the Jeeni is running version 2.2 firmware or later. The firmware is available from the EPI's web site <a href="http://www.epitools.com/">http://www.epitools.com/</a>.
- 2. Use the ejconfig program to configure the Jeeni to assert the nSRST signal until the start of the debug session. The ejconfig program is shipped with the Jeeni. It is also available for download from EPI's web site. When you run ejconfig, it will prompt you for the Jeeni's IP address, and then ask a series of questions. When ejconfig asks if the Jeeni should assert nSRST, answer "yes". Accept the defaults for all other questions, including those about the timing of the nSRST signal.

Once the Jeeni has been reconfigured, it will hold the processor in reset until the debug session actually starts. This guarantees that it will get control of the processor, even if it has executed illegal instructions.

Customers who have boards that followed the old design guidelines should update them to follow the design above, if possible. If it is not possible to patch the existing boards, then the following procedure will usually gain control of the boards that use the old design, even if flash is corrupted.

- 1. Make sure the Jeeni is running version 2.2 firmware or later.
- 2. Make sure the Jeeni is NOT configured to assert nSRST. Asserting this signal on boards that follow the old design guidelines will prevent the Jeeni from gaining control.
- 3. Power up the Jeeni and the board at the same time.
- 4. Try to start a debug session as normal.
- 5. If the Jeeni is not able to get control of the board, then terminate the debug and rdisery sessions.
- 6. Push the reset button on the Jeeni.
- 7. Restart the debug session. The Jeeni should be able to get control of the board at this point.

Customers who have a mixture of boards with the old JTAG and new JTAG interface designs should use the above procedure for both types of boards. This is because asserting nSRST on a board that follows the old design will prevent the Jeeni from gaining control of it. However, the Jeeni can usually gain control of either board type after its reset button is pushed.

We apologize for any inconvenience this may cause.