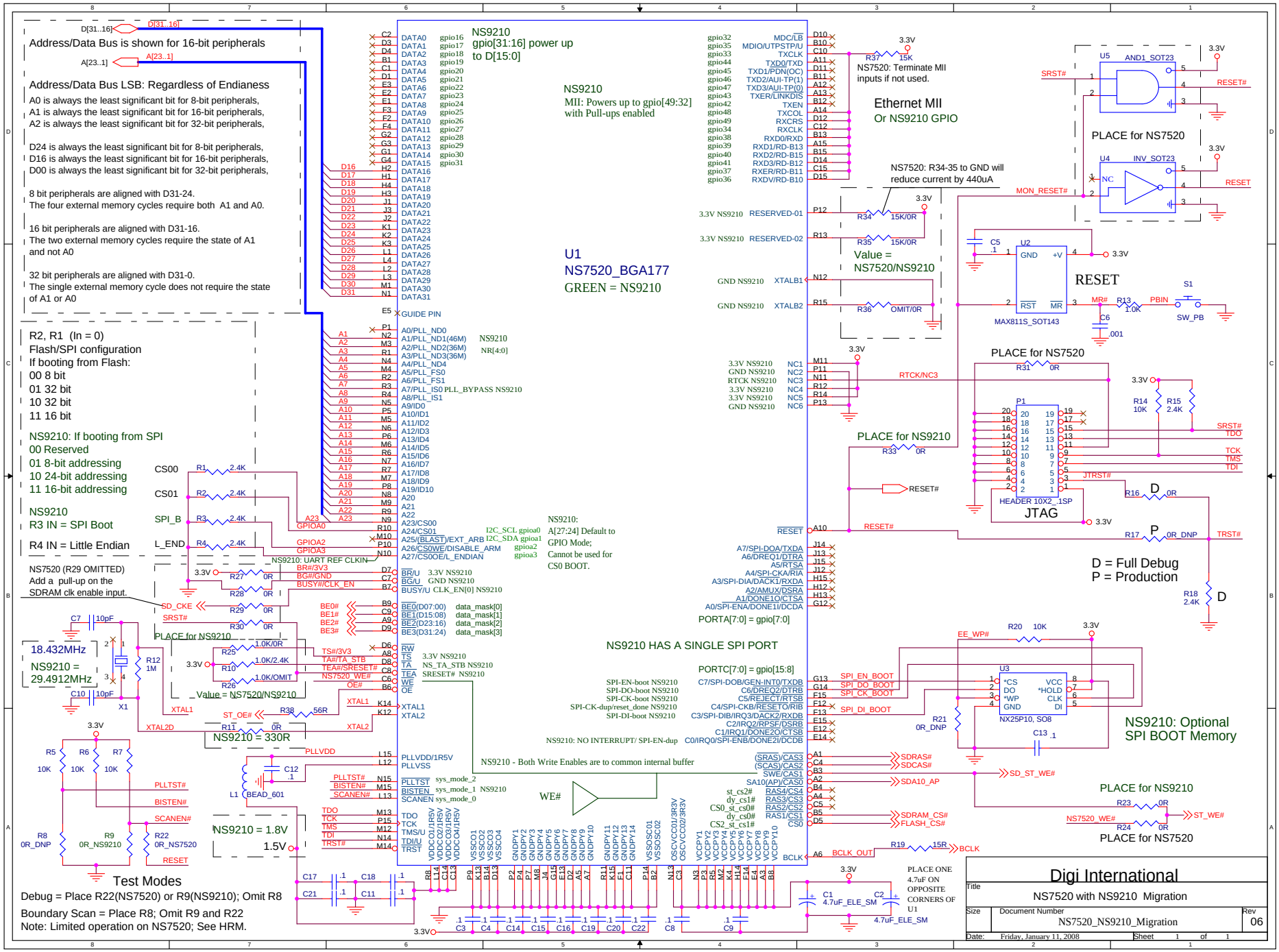
Address/Data Bus is shown for 16-bit peripherals
Address/Data Bus LSB: Regardless of Endianess
A0 is always the least significant bit for 8-bit peripherals,
A1 is always the least significant bit for 16-bit peripherals,
A2 is always the least significant bit for 32-bit peripherals,
D24 is always the least significant bit for 8-bit peripherals,
D16 is always the least significant bit for 16-bit peripherals,
D00 is always the least significant bit for 32-bit peripherals,
8 bit peripherals are aligned with D31-24.
The four external memory cycles require both A1 and A0.
16 bit peripherals are aligned with D31-16.
The two external memory cycles require the state of A1 and not A0
32 bit peripherals are aligned with D31-0.
The single external memory cycle does not require the state of A1 or A0
R2, R1 (In = 0)
Flash/SPI configuration
If booting from Flash:
00 8 bit
01 32 bit
10 32 bit
11 16 bit
NS9210: If booting from SPI
00 Reserved
01 8-bit addressing
10 24-bit addressing
11 16-bit addressing
NS9210
R3 IN = SPI Boot
R4 IN = Little Endian
NS7520 (R29 OMITTED)
Add a pull-up on the SDRAM clk enable input.
18.432MHz
NS9210 = 29.4912MHz
NS9210 = 330R
NS9210 = 1.8V
1.5V
Test Modes
Debug = Place R22(NS7520) or R9(NS9210); Omit R8
Boundary Scan = Place R8; Omit R9 and R22
Note: Limited operation on NS7520; See HRM.
NS9210
gpio[31:16] power up to D[15:0]
NS9210
MII: Powers up to gpio[49:32] with Pull-ups enabled
U1
NS7520_BGA177
GREEN = NS9210
NS9210:
A[27:24] Default to GPIO Mode;
Cannot be used for CS0 BOOT.
NS9210 HAS A SINGLE SPI PORT
NS9210 - Both Write Enables are to common internal buffer
NS9210: NO INTERRUPT/ SPI-EN-dup
NS7520: Terminate MII inputs if not used.
Ethernet MII
Or NS9210 GPIO
NS7520: R34-35 to GND will reduce current by 440uA
Value = NS7520/NS9210
PLACE for NS7520
RESET
MAX811S_SOT143
PLACE for NS7520
PLACE for NS9210
HEADER 10X2_.1SP
JTAG
D = Full Debug
P = Production
NS9210: Optional SPI BOOT Memory
NX25P10, SO8
PLACE for NS9210
PLACE for NS7520
PLACE ONE 4.7uF ON OPPOSITE CORNERS OF U1
Digi International
Title
NS7520 with NS9210 Migration
Size
Document Number
NS7520_NS9210_Migration
Rev
06
Date: Friday, January 11, 2008
Sheet 1 of 1