GPIO[07:00]

Serial Port A

GPIO[58:51]

Serial Port B

GPIO[15:08]

Serial Port C

GPIO[12] defaults to RESET_DONE
(Output Low to high)

GPIO[103:59]

Port D_gpio[66:59]
FIM_0/1_BUS[23:16]
for external Interrupts
<<Or Serial Port D>>

Port E_gpio[75:68]
GPIO only

Port F_gpio[87:80]
FIM_0/1_BUS[07:00]
for external Interrupts

Port G_gpio[95:88]
FIM_0/1_BUS[15:08]
for external Interrupts

Port H_gpio[103:96]
FIM_0/1_BUS[07:00]
for external Interrupts

SERIAL PORT A
RI# ON PORT C

SERIAL PORT B
RI# ON PORT C

MISC. PORT C

PORT D

PORT E

ENI/MIC PORT GPIO MODE

PORT F

PORT G

PORT H

U1_BEFORE
NET+50_BGA208

ADDRESS BUS

DATA BUS

CONTROL BUS

MII

BS_ENDIAN

BS_BW1

See HRM for bootstrap information

A[23:0]

D[31:0]

DQM3#
DQM2#
DQM1#
DQM0#

SD_CLK

SD_CKE

SD_RAS#
SD_CAS#
SD_A10
SD_ST_WE#
SD_ST_OE#

TA_STB

FLASH_CS#
SDRAM_CS#

UNUSED ADC

See HRM for using ADC

SYSTEM MODE - POR Disabled
Debug: populate R27; omit R29
Boundary Scan: populate R29; omit R27

U1_AFTER
NS9215_BGA265

SYSTEM

3V3_IO

VCORE

GNDS

10 - 3V3_IO
TO
17 - 3V3_IO

4 - 2V5
TO
11- 1V8
VCORE

14 GND PINS
TO
22 GND PINS

MII[18:00]

RESET IN FROM POWER MONITOR

JTAG

HEADER 10X2_1SP

SRESET#
TDO
RTCK
TCK
TMS
TDI
TRST#

0-220R for Production
and no debug

1V8_PLL

See HRM for using internal POR
and/or RTC

To Ethernet PHY

MII[18:0]

MII18 is an interrupt in from the PHY, or it can be general purpose.

Digi International	
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