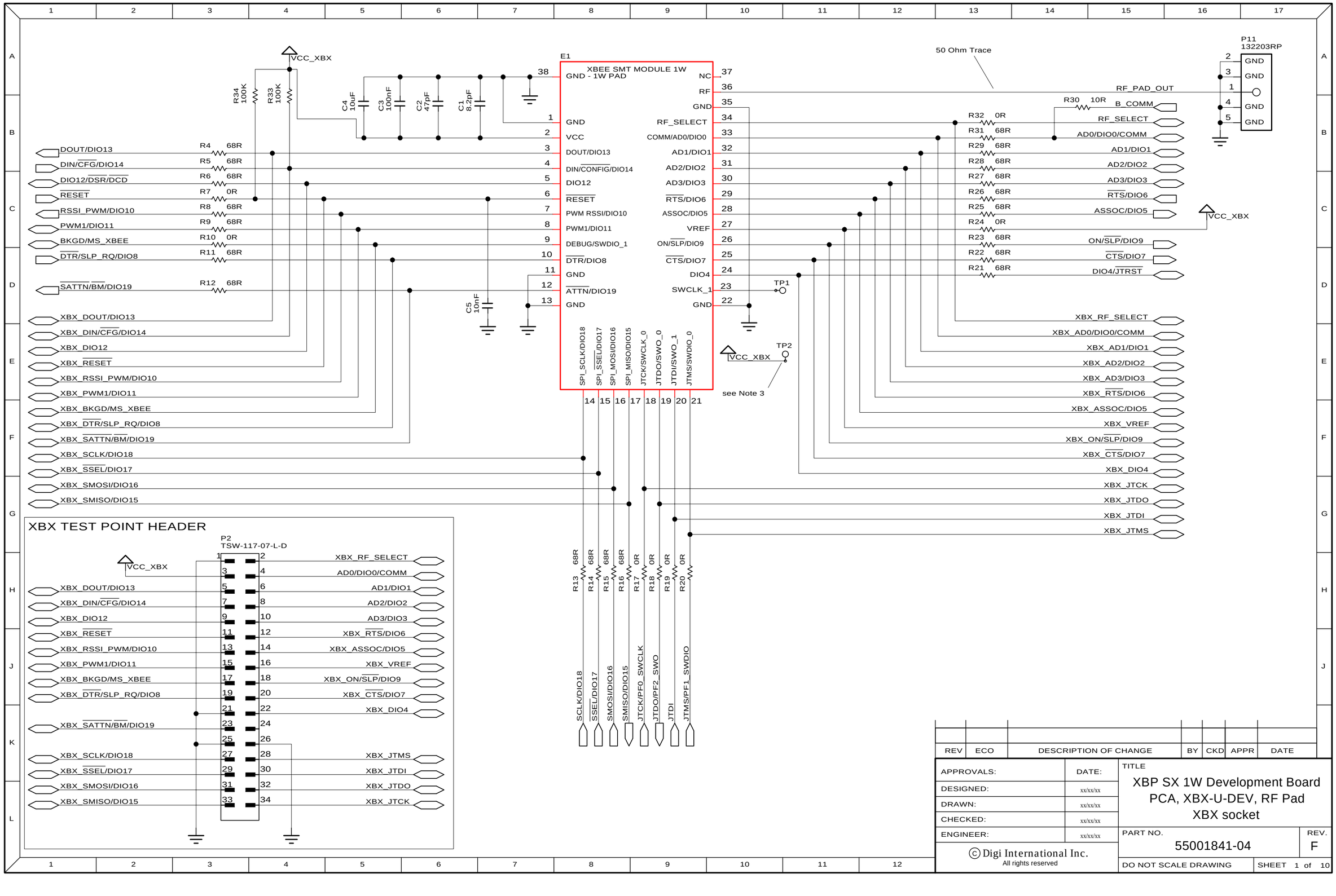


REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
XBX socket

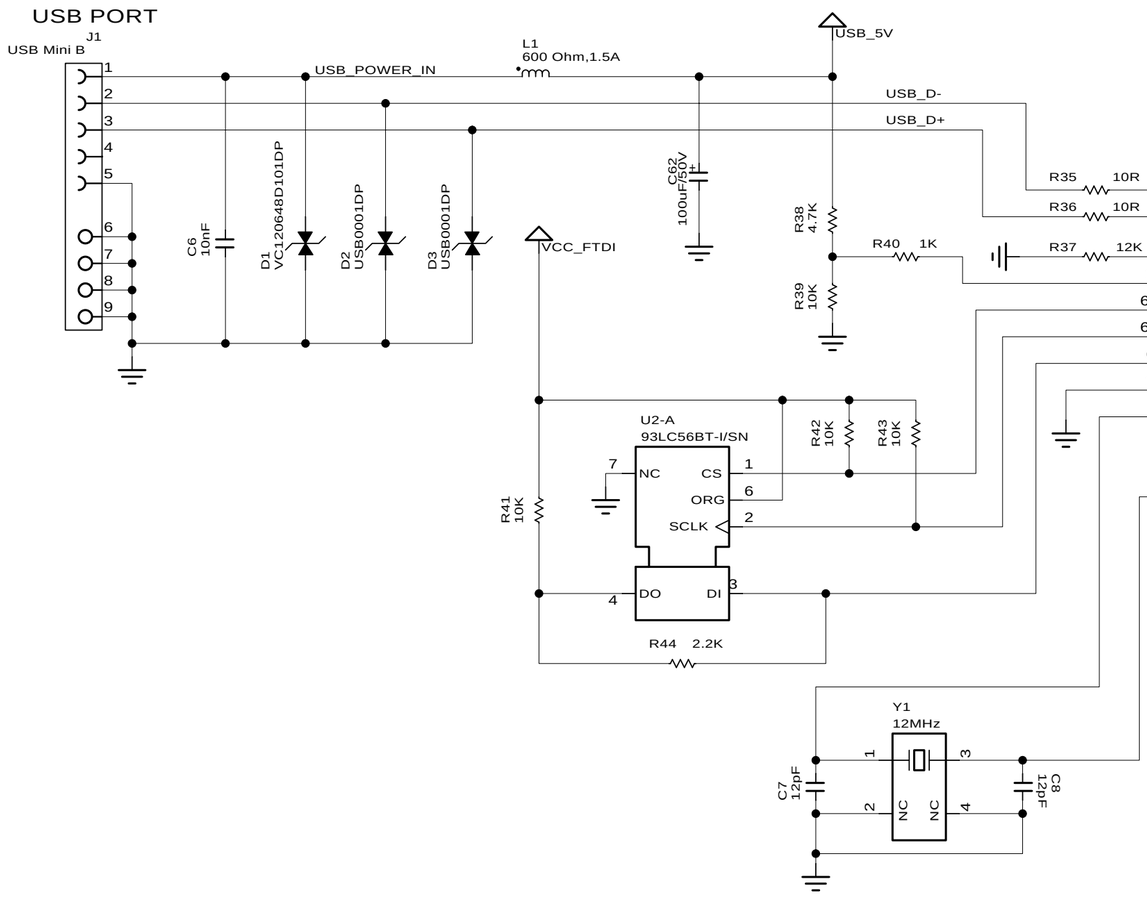
PART NO. 55001841-04

REV. F

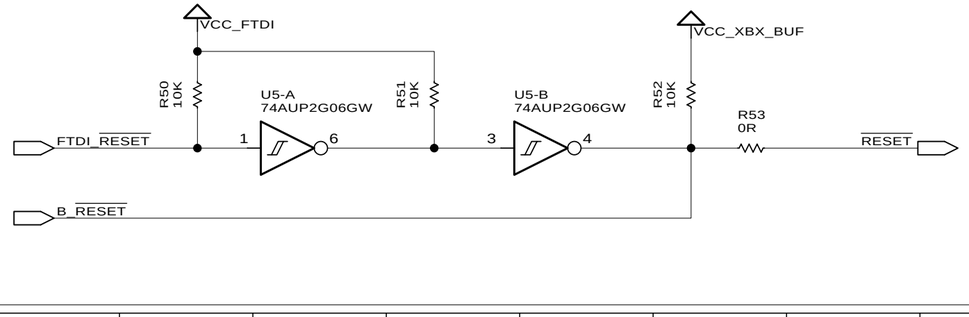
DO NOT SCALE DRAWING

SHEET 1 of 10

USB PORT



RESET



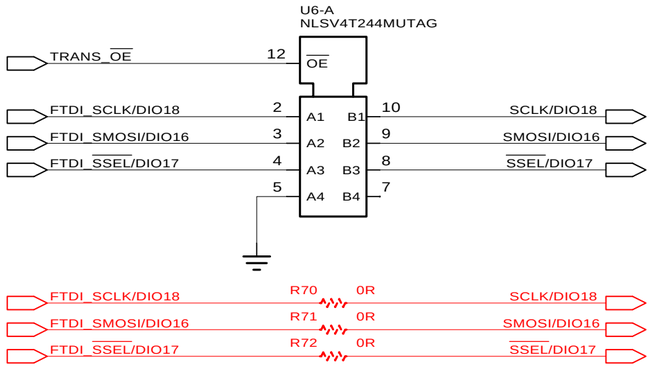
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

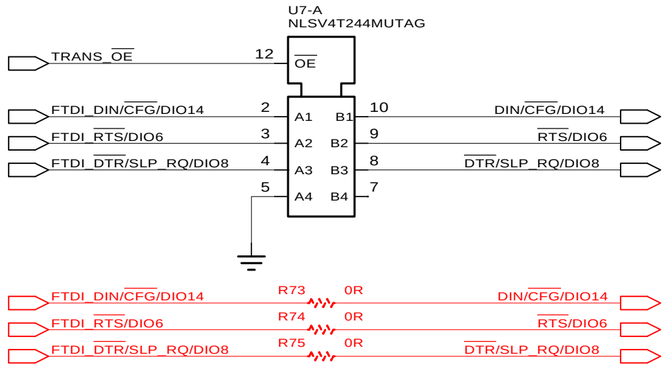
APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

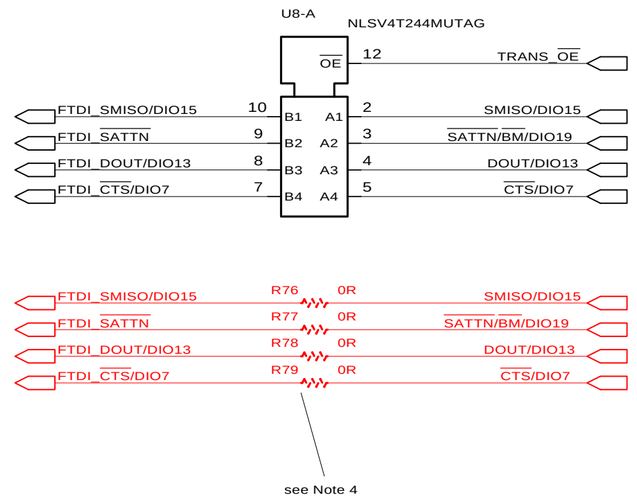
TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
USB, FTDI, and RESET

PART NO. 55001841-04 REV. F

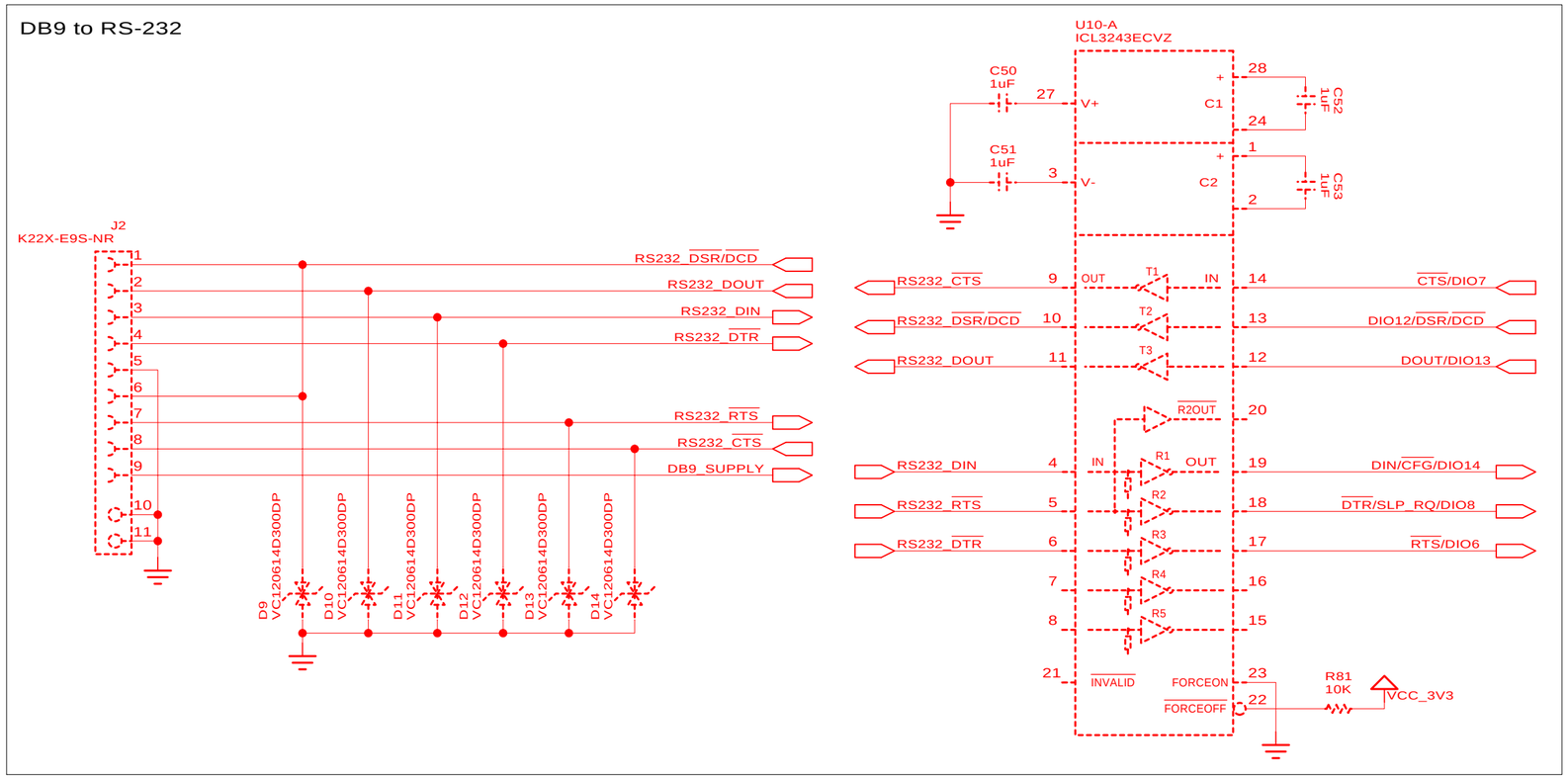
DO NOT SCALE DRAWING SHEET 2 of 10







The FTDI chip will control both the UART and SPI lines over the entire XBee Voltage range due to these unidirectional translators. If GPIO testing is desired, the NI I/O control device must be used.



The RS-232 transceiver will only be used on the certifications variant. The regulator, FTDI chip, translators, and all other unnecessary components will be removed. This will allow the certification lab to accurately test the module.

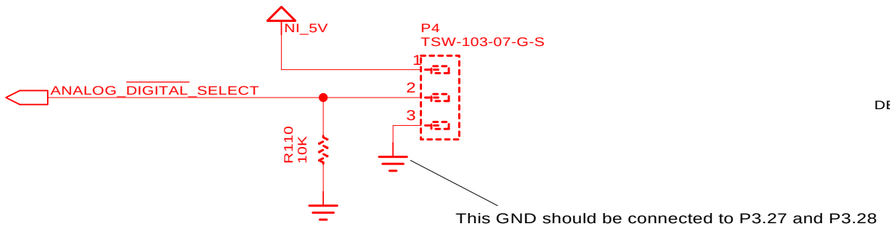
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
FTDI I/O and DB9 Connections

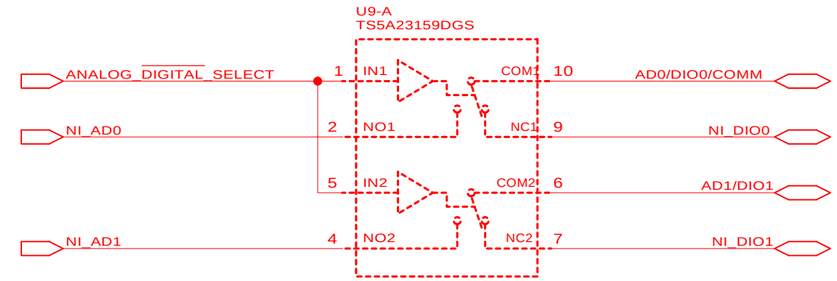
PART NO. 55001841-04 REV. F

DO NOT SCALE DRAWING SHEET 3 of 10



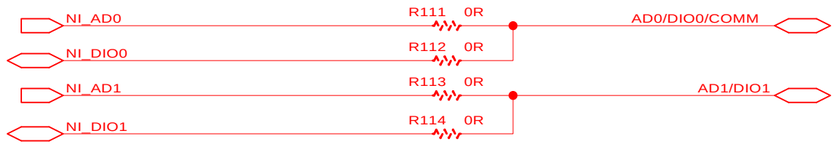
J3
390088-02

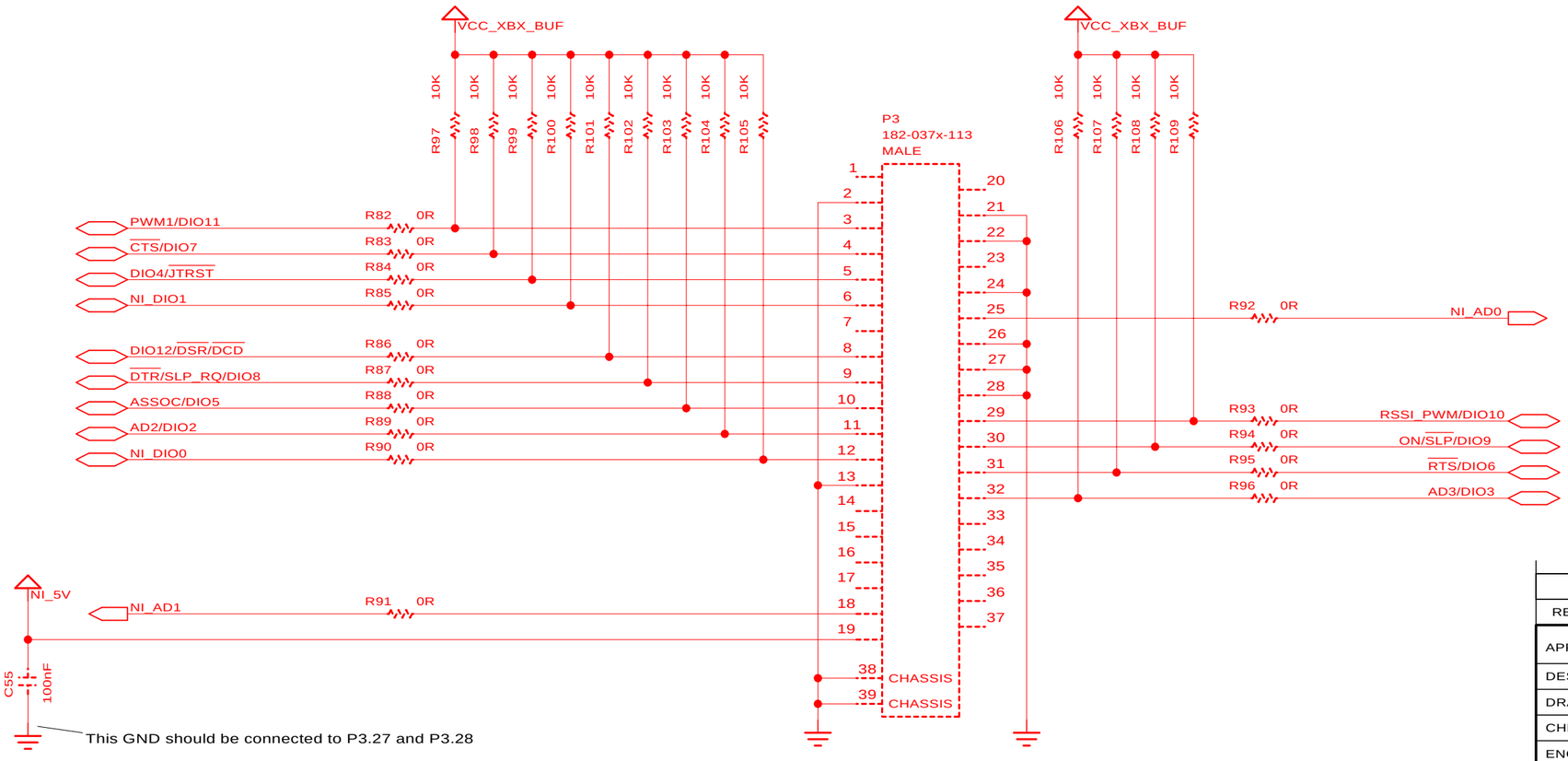
DEFAULT PLACED ON PINS 2 AND 3 OF P4



The NI I/O Control Device (USB-6003) is capable of testing up to 13 DIO lines and 2 AO lines. This device will be used to perform all analog and digital I/O testing.

The U9 analog switch will determine whether the digital or analog lines will be tested. When the select line is high, the analog lines will be tested. When the select line is low, the digital lines will be tested. The default will be digital.





REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

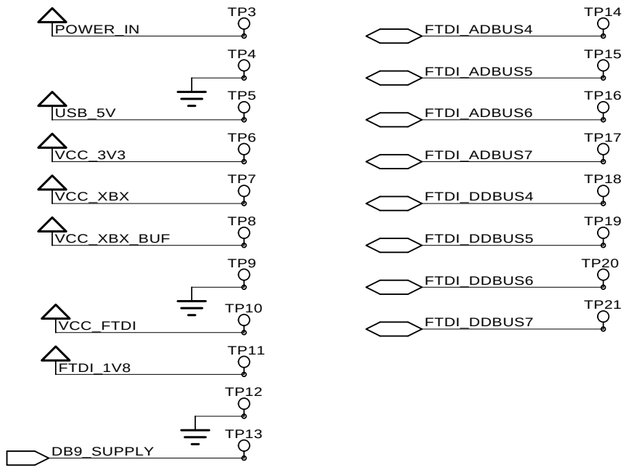
APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
NI Device I/O Connections

PART NO. 55001841-04
REV. F

DO NOT SCALE DRAWING
SHEET 4 of 10

TEST POINTS



- Label TP3 "Power In" and TP4 as "GND". Place them near P7.

- Label TP5 "USB 5V" and place it near J1.

- Label TP6 "3.3V" and place near P5 and P6.

- Label TP7 "VCC XBX" and place near the XBX module.

- Label TP8 "VCC XBX BUFF" and place it anywhere.

- Label TP9 "GND" and place it near TP7.

- Label TP10 "VCC FTDI", TP11 "1.8V", and TP12 "GND". Place them near U1.

- Label TP13 "DB9 VCC" and place near J2.

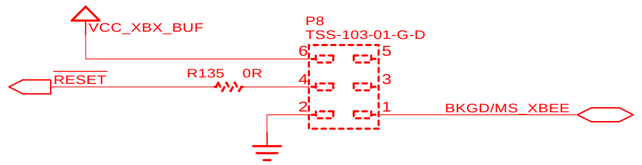
- Place TP14-TP21 near U1

- Label TP14-TP17 as "A4" - "A7"

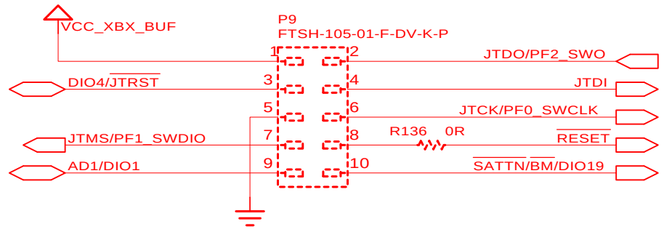
- Label TP18-TP21 as "D4" - "D7"

HEADERS

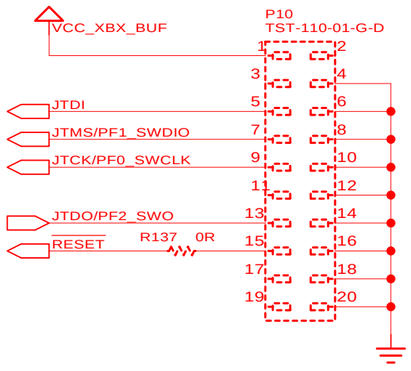
CYCLONE PROGRAMMING



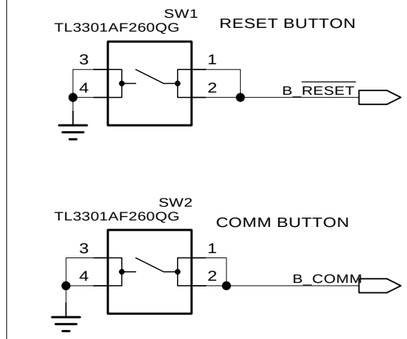
EMBER/INSIGHT



JTAG SEGGER



BUTTONS



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

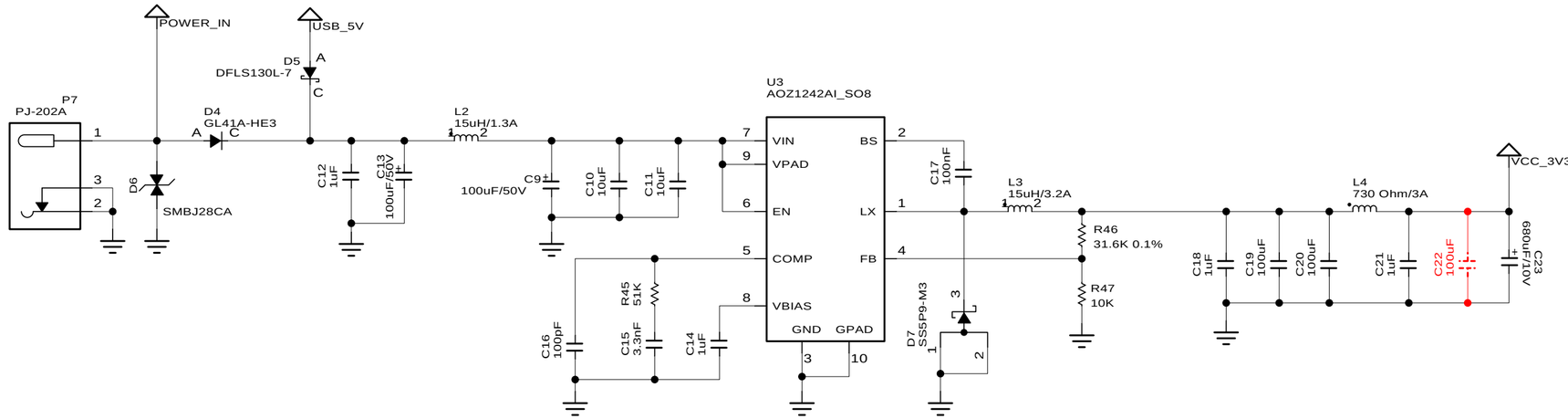
TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
Headers, Switches, and Test Points

PART NO. 55001841-04

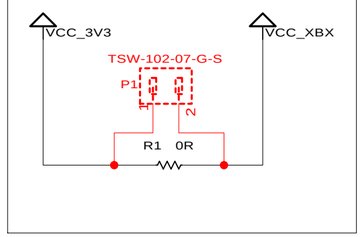
REV. F

DO NOT SCALE DRAWING

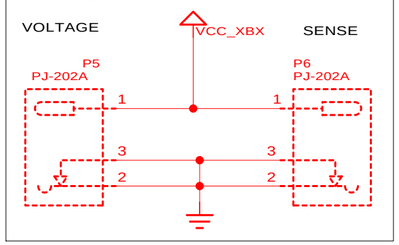
3.3V SWITCHING REGULATOR



CURRENT TESTING

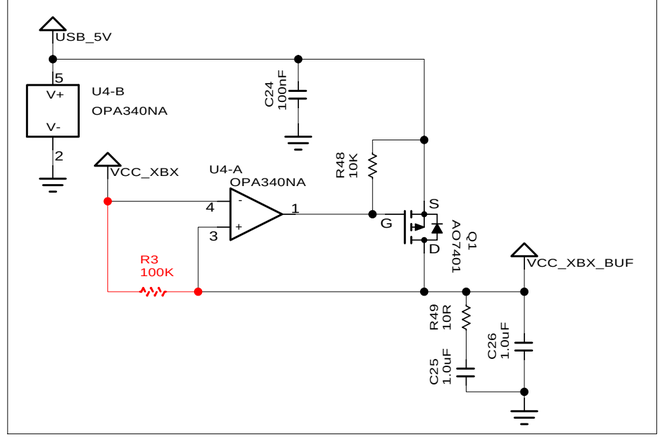


Sensing Power Supply

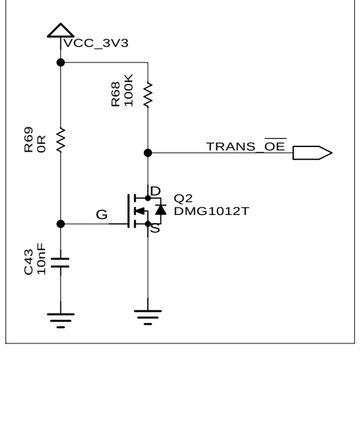


FTDI VCC

VCC XBEE BUFFER



$\overline{\text{OE}}$ INVERTER



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

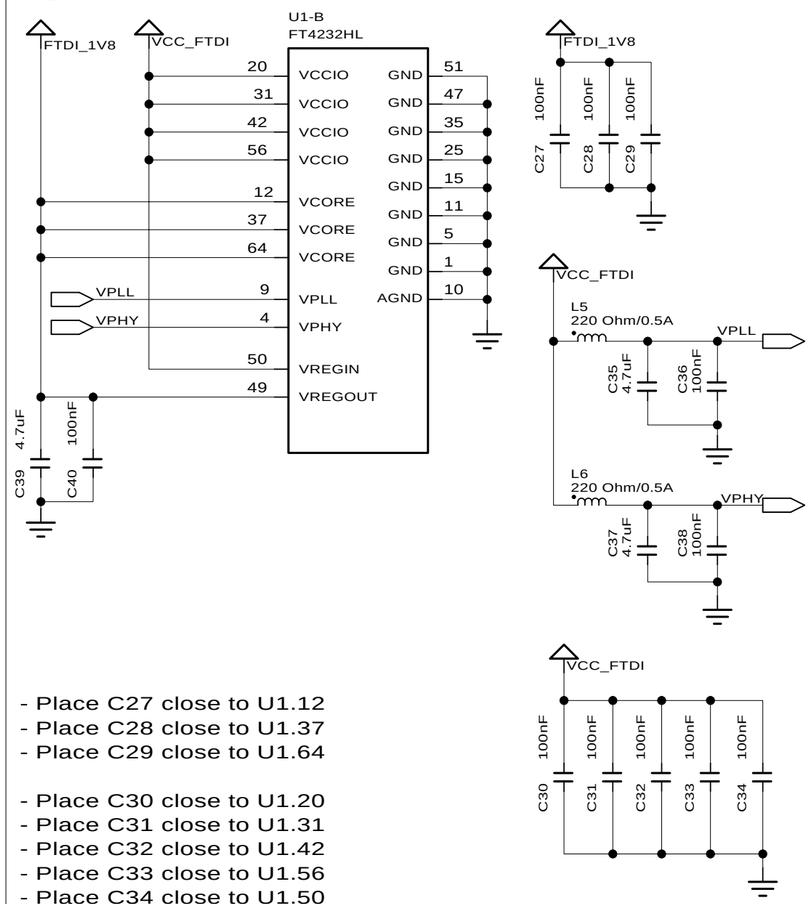
APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE: XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
Power - Supplies

PART NO. 55001841-04 REV. F

DO NOT SCALE DRAWING SHEET 6 of 10

FTDI CHIP



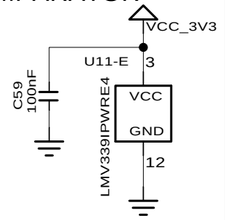
- Place C27 close to U1.12
- Place C28 close to U1.37
- Place C29 close to U1.64

- Place C30 close to U1.20
- Place C31 close to U1.31
- Place C32 close to U1.42
- Place C33 close to U1.56
- Place C34 close to U1.50

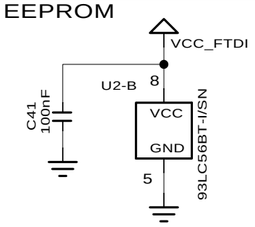
- Place C35 and C36 close to U1.9
- Place C37 and C38 close to U1.4

- Place C39 and C40 close to U1.49

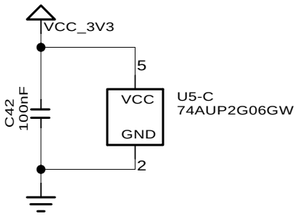
COMPARATOR



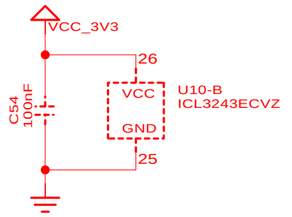
EEPROM



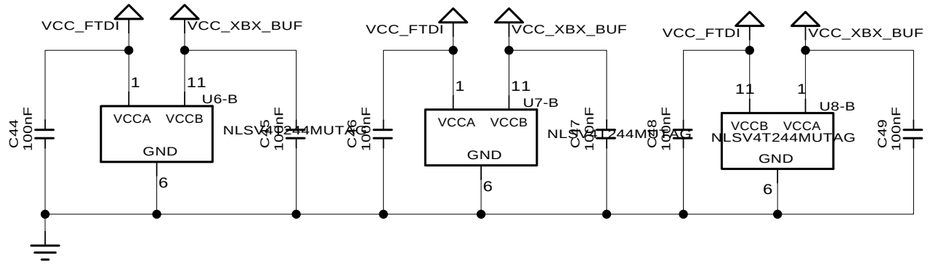
RESET INVERTER



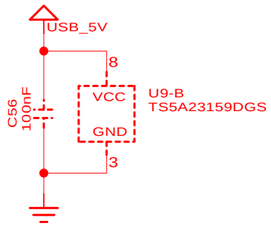
DB9 to RS232



TRANSLATORS



NI ANALOG SWITCH



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
Power - Chips

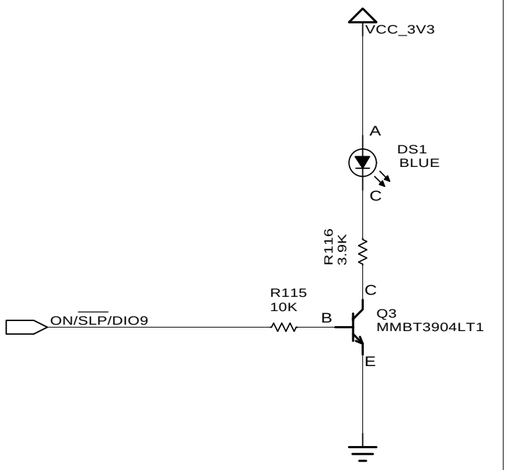
PART NO. 55001841-04

REV. F

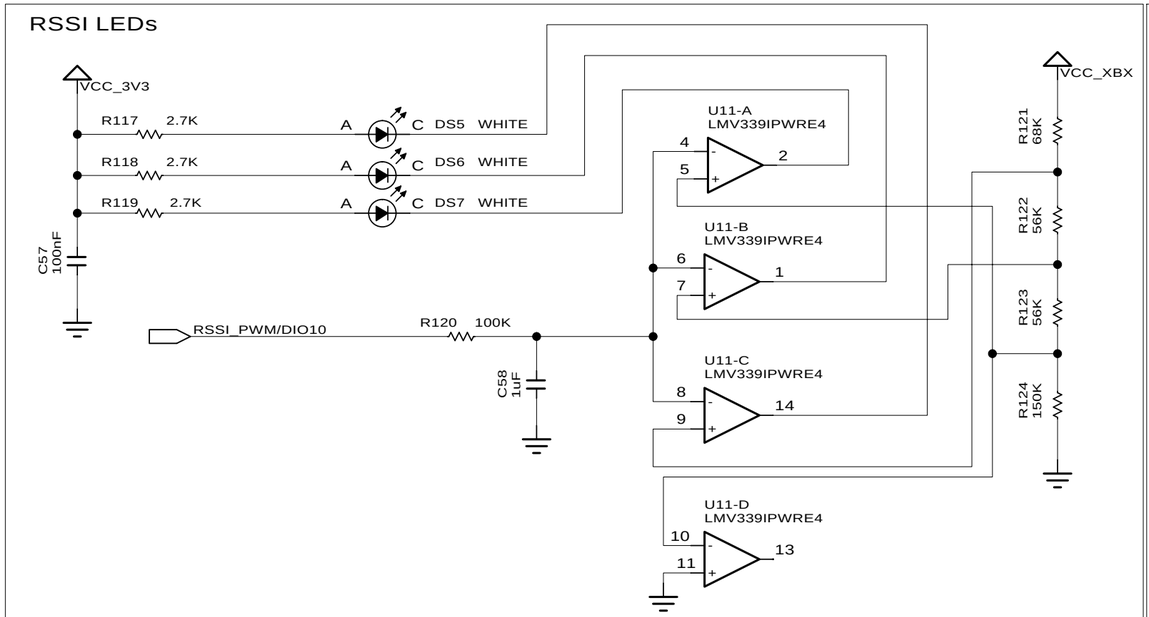
DO NOT SCALE DRAWING

SHEET 7 of 10

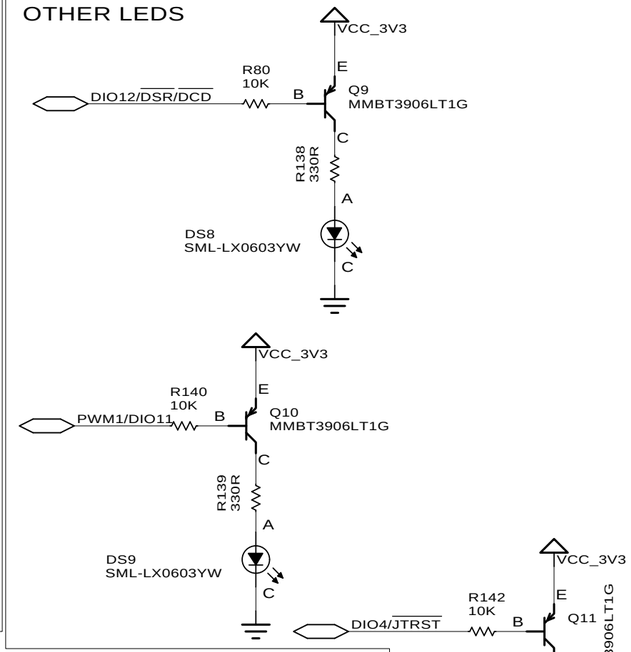
ON/SLEEP LED



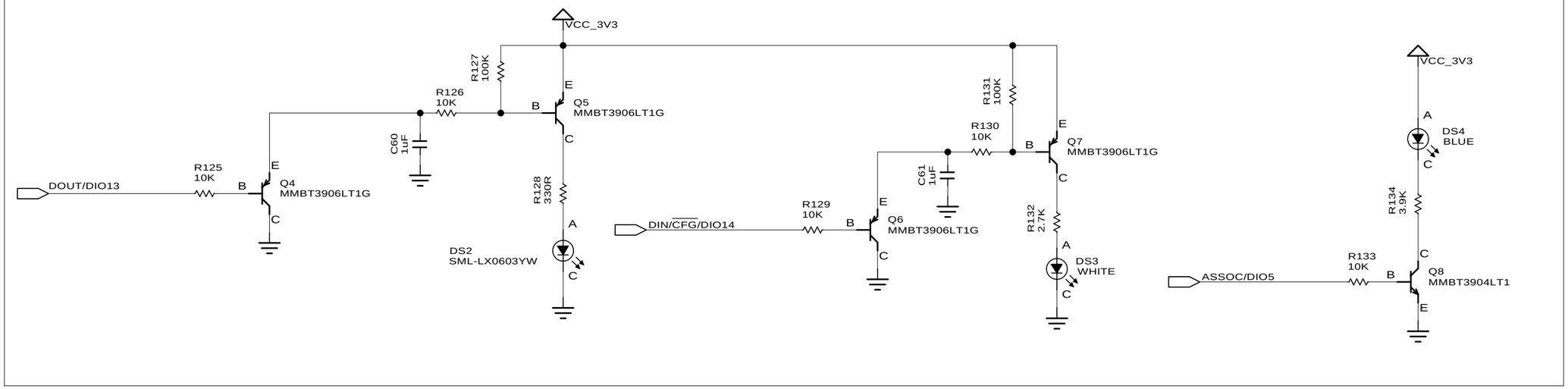
RSSI LEDs



OTHER LEDS



DOUT, DIN, AND ASSOC LEDS



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
LEDs

PART NO. 55001841-04

REV. F

DO NOT SCALE DRAWING

Notes

1. The FT4232H chip has 4 separate I/O ports. Each of these ports can be set to different modes at any time. Only one mode can be set on a port at a time. All of the ports can be set to serial, asynchronous bit-bang, or synchronous bit-bang. Only ports A and B can be set to MPSSE mode, which includes SPI, I2C, and JTAG modes. The default state for all of the ports will be UART whenever plugged in. This cannot be changed.

2. The FT4232H chip supports two modes for the SPI clock. The first mode supports speeds from 92 Hz to 6 MHz and follows the equation below (CD is the clock divisor and must be an integer:

   f = 12MHz / (2 * (1 + CD))

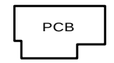
   The other mode can handle speeds between 460 Hz and 30 MHz and follows the equation below:

   f = 60 MHz / (2 * (1 + CD))

   The MOSI and MISO lines are synchronous with the SPI clock. All of the other GPIO pins are not.

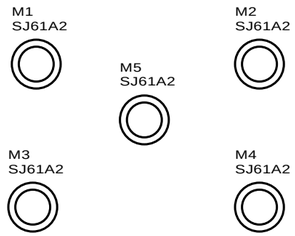
3. Place TP1 and TP2 next to each other in an 0603 layout (within 60 mil of each other).

PCB1
30009462-03

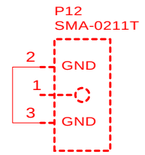


E2
30009468-03

Rubber feet



U.FL to SMA



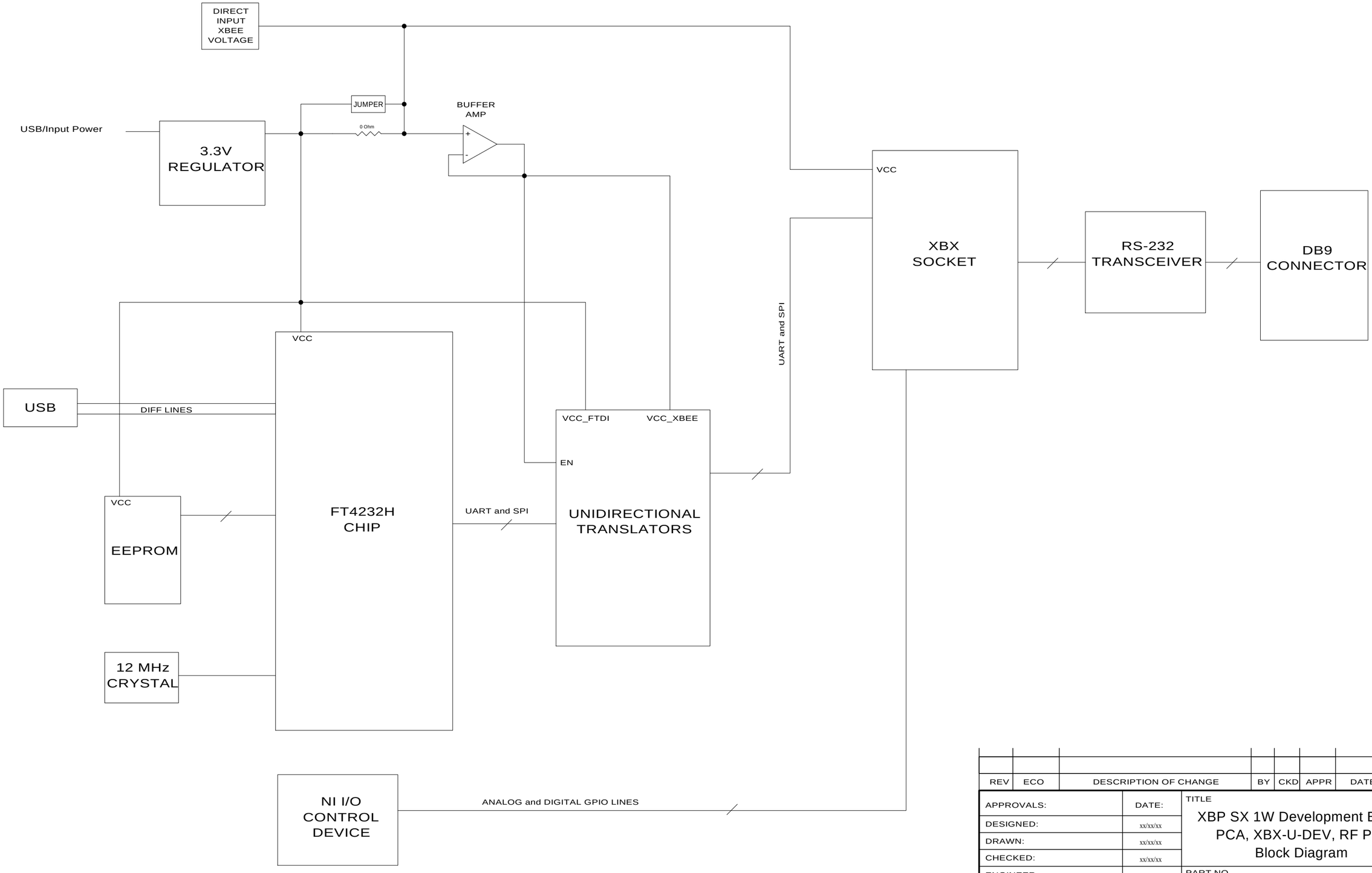
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
Notes and Mechanicals

PART NO. 55001841-04 REV. F

DO NOT SCALE DRAWING



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:
DESIGNED:	xx/xx/xx
DRAWN:	xx/xx/xx
CHECKED:	xx/xx/xx
ENGINEER:	xx/xx/xx

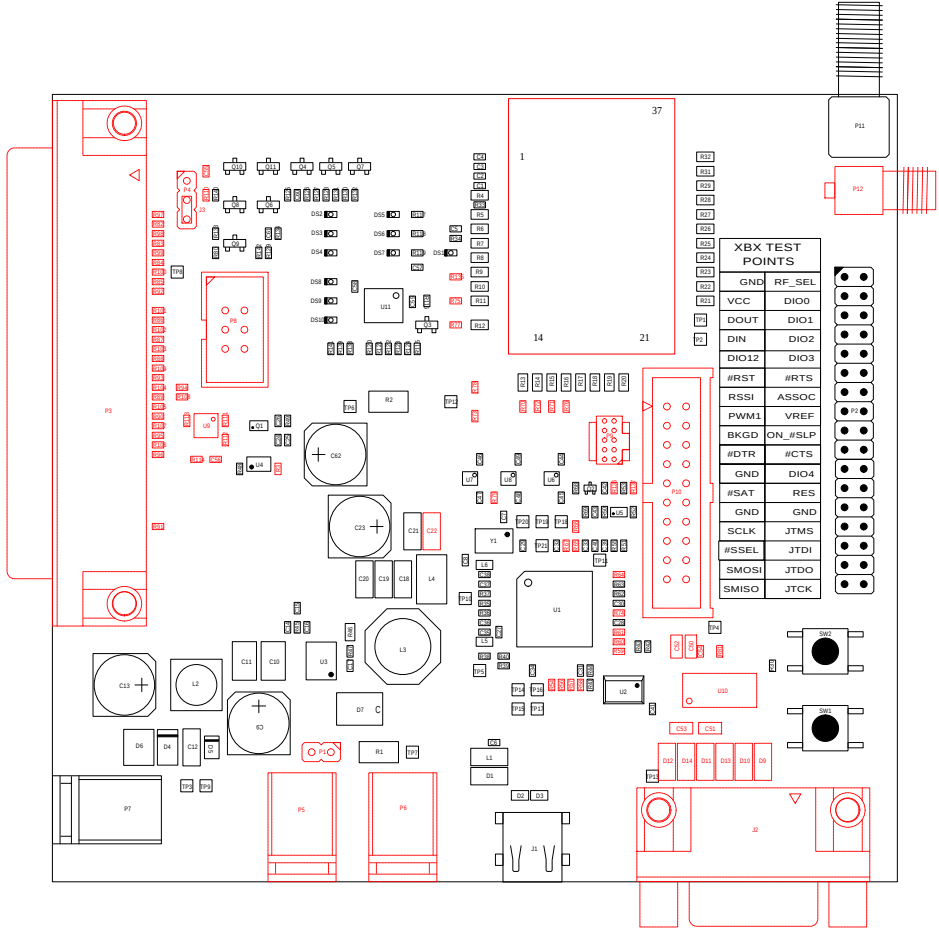
TITLE
XBP SX 1W Development Board
PCA, XBX-U-DEV, RF Pad
Block Diagram

PART NO. 55001841-04

REV. F

DO NOT SCALE DRAWING

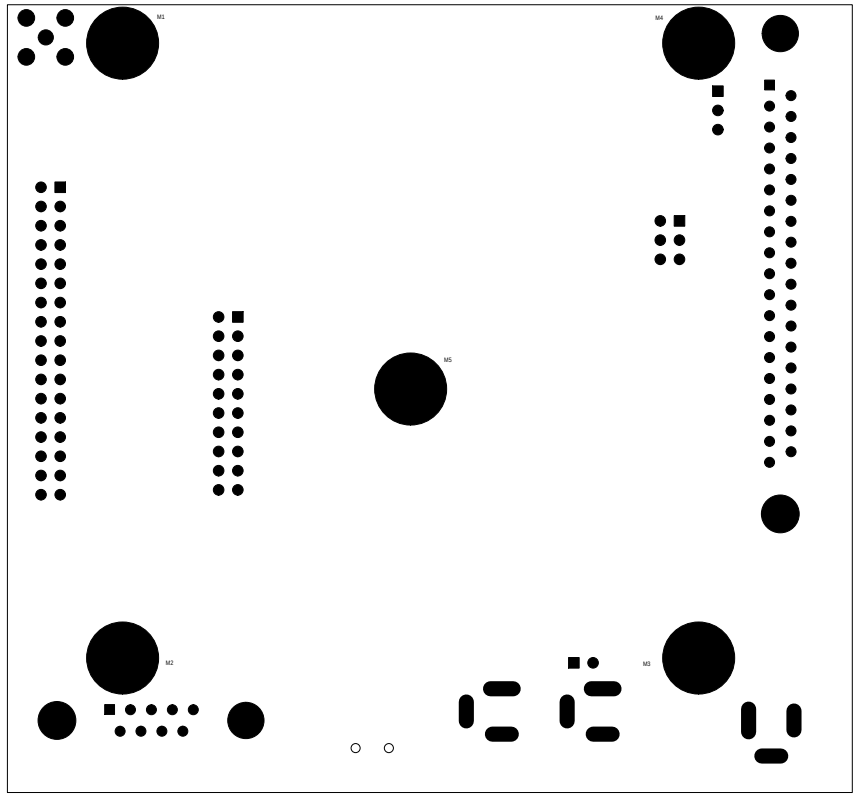
SHEET 10of 10



XBX TEST POINTS	
GND	RF_SEL
VCC	DIO0
DOUT	DIO1
DIN	DIO2
DIO12	DIO3
#RST	#RTS
RSSI	ASSOC
PWM1	VREF
BKGD	ON_#SLP
#DTR	#CTS
GND	DIO4
#SAT	RES
GND	GND
SCLK	JTMS
#SSEL	JTDI
SMOSI	JTDO
SMISO	JTCK

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:	DIGI INTERNATIONAL MINNETONKA, MN 55343	
DESIGNED:		TITLE	
DRAWN:		Top Assembly	
CHECKED:		PCA, XBX-U-DEV, RF Pad	
ENGINEER:		PART NO.	REV.
UNLESS OTHERWISE SPECIFIED: TOL: .xx=+/-.010" .xxx=+/-.005"		55001841-04	F
		DO NOT SCALE DRAWING	SHEET 1 of 2



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

APPROVALS:	DATE:	DIGI INTERNATIONAL MINNETONKA, MN 55343	
DESIGNED:		TITLE	
DRAWN:		Bottom Assembly	
CHECKED:		PCA, XBX-U-DEV, RF Pad	
ENGINEER:		PART NO.	REV.
UNLESS OTHERWISE SPECIFIED: TOL: .xx=+/-.010" .xxx=+/-.005"		55001841-04	F
		DO NOT SCALE DRAWING	SHEET 2 of 2