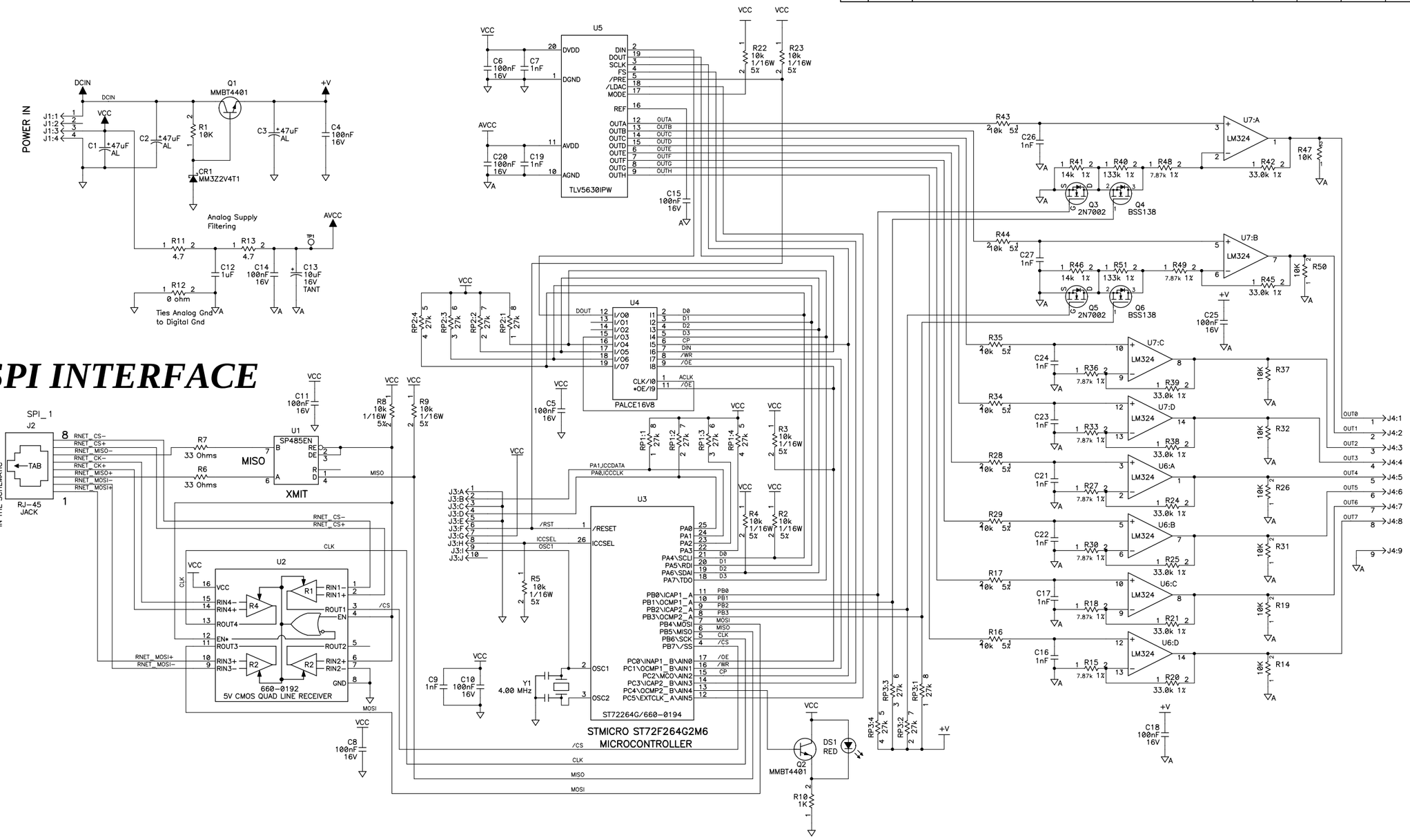
REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION OF CHANGE	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
A	E12356	INITIAL RELEASE	VO	7/25/03	KF	7/25/03

SPI INTERFACE



NOTES: UNLESS OTHERWISE SPECIFIED;

1. ALL RESISTOR VALUES ARE IN OHMS, 1/16W 0603 PACKAGE, 5%
2. ALL CAPACITORS ARE 50VDC OR HIGHER.
3. THE ORIGINATION SOURCE OF A VOLTAGE IS REPRESENTED BY (VCC), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY (VCC).

4 OUTLINED CIRCUIT MAY NOT BE STUFFED DEPENDING ON MODEL, SEE STUFFING CHART FOR CLARIFICATION.

5. COMPONENT VALUES SHOWN WITH AN ASTERISK (*) FOLLOWING THE VALUE, MAY HAVE DIFFERENT VALUES, OR MAY NOT BE STUFFED DEPENDING ON MODEL. SEE STUFFING CHART FOR CLARIFICATION.

Power Table						
Ref Des	Device(Type)	Package	GND	+V	VCC	AGND
U1	660-0191	SOIC-8B	5		8	
U3	660-0194	SOP28-300	27		28	
U4	652-0002	652-0002	10		20	
U6	660-0140	660-0140		4		11
U7	660-0140	660-0140		4		11

APPEND THE FOLLOWING DOCUMENTS WHEN CHANGING THIS DOCUMENT:

DRAWING CONTENT:

DRAWN BY: (INITIAL RELEASE) J. FENG/VAN 7/25/03

REVISED BY:

APPROVALS: INITIAL RELEASE

PROJECT ENGINEER:

ENGINEERING MANAGER:

SIGNATURES DATE

TITLE

SCHEMATIC DIAGRAM
RABBITNET
RN1300 DAC BOARD

Z-WORLD
2900 SPAFFORD ST.
DAVIS, CA 95616
530 - 757-4616

SIZE C

DWG NO. 090-0179

SCALE NONE

RELEASE DATE

SHEET 1 OF 1