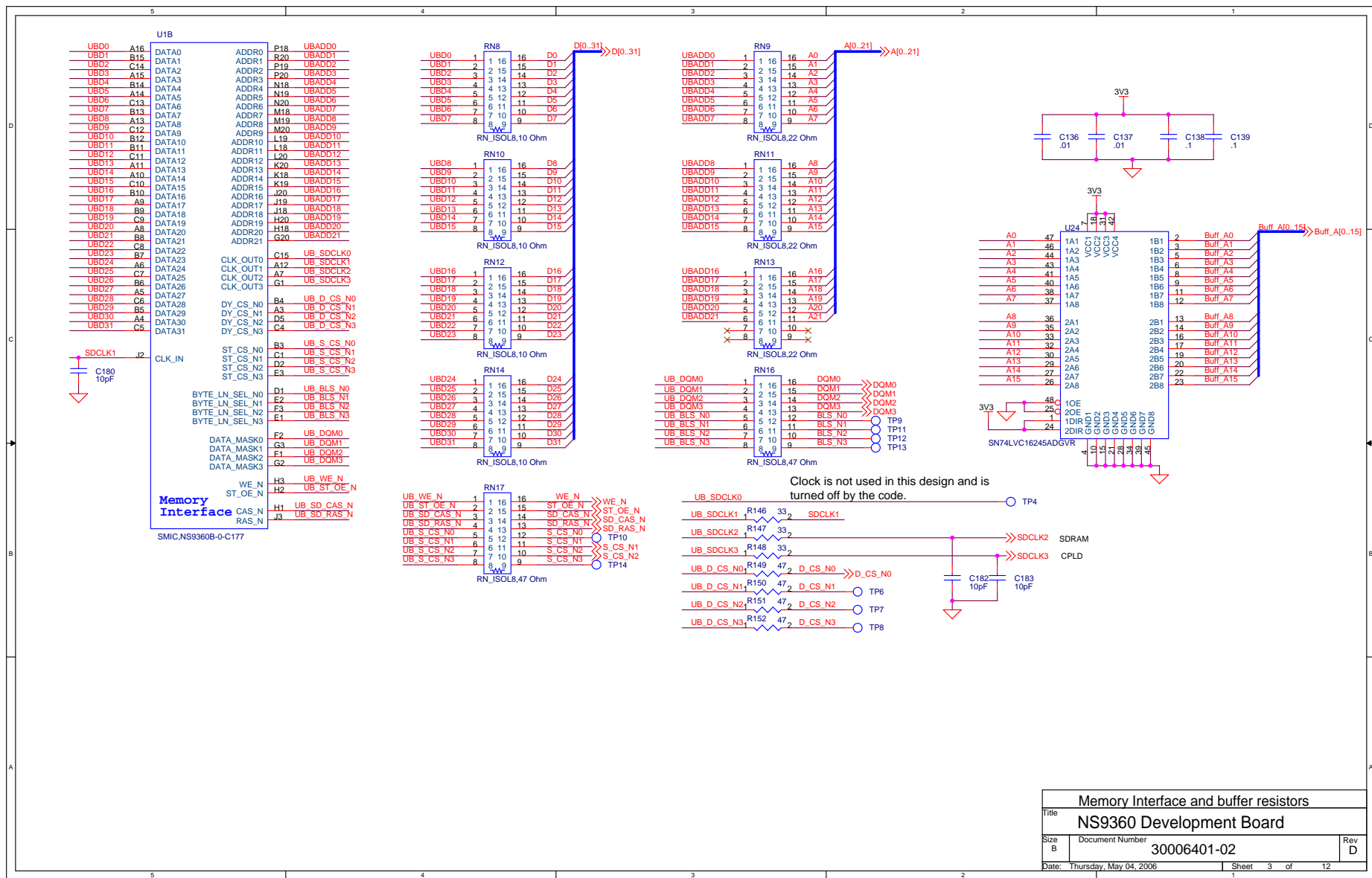


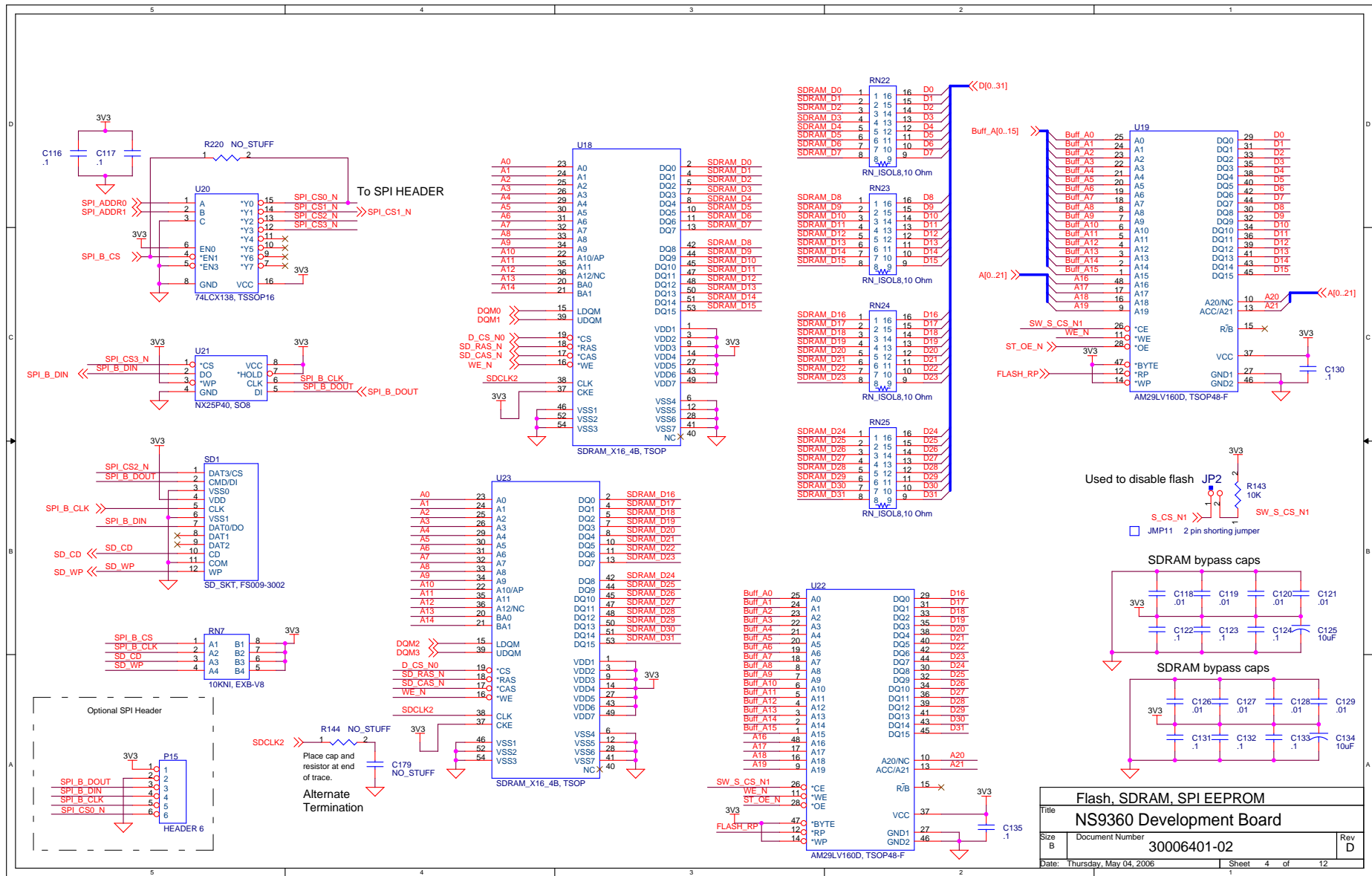
X2 and Y1 are double footprinted. Pins 2 and 3 are shared by both. Populating according to * and ** (astericks) isolates each.

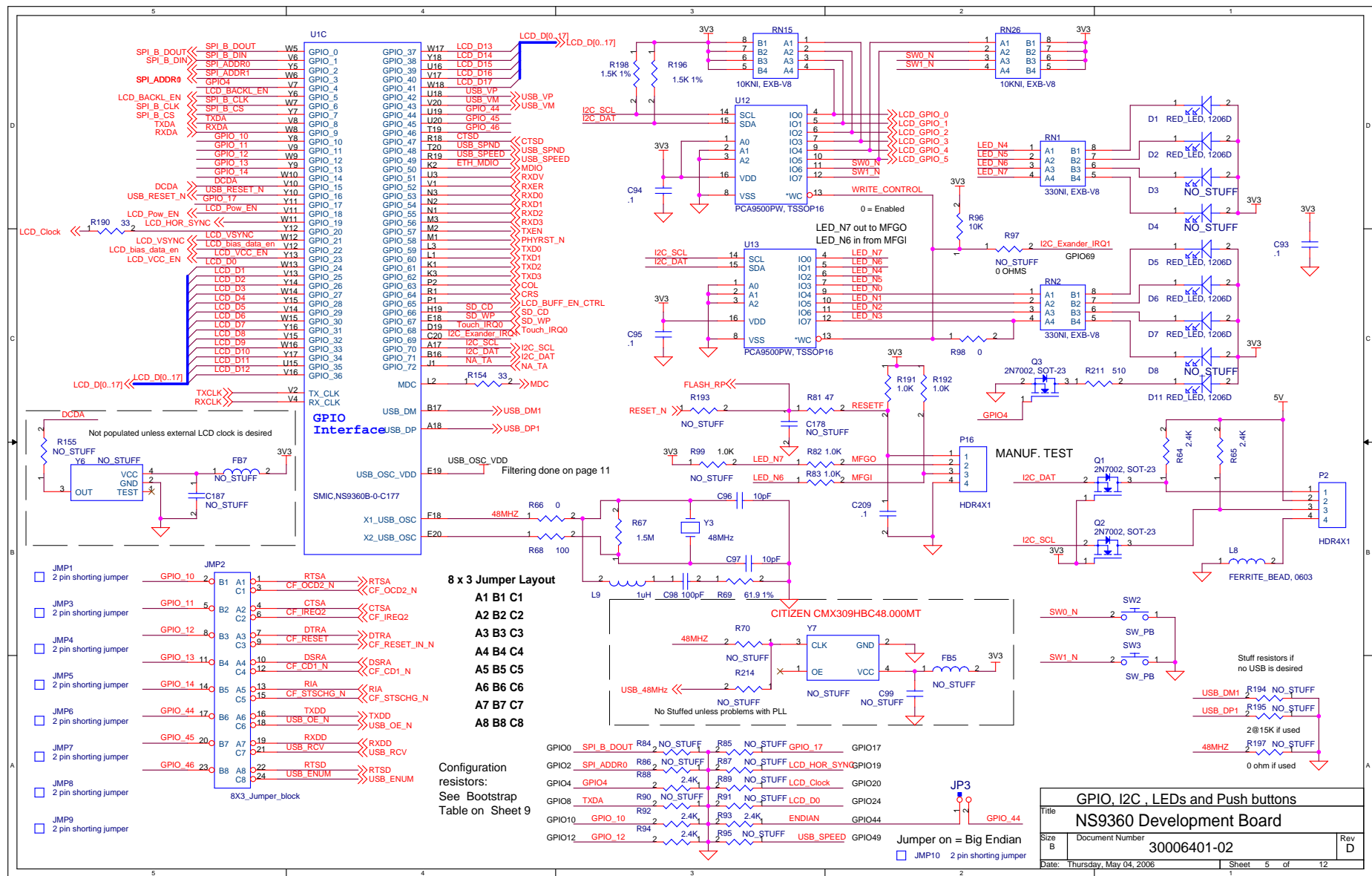
** = Populated when using PLL and Crystal(X2).
* = Populated when using PLL with OSC(Y1).

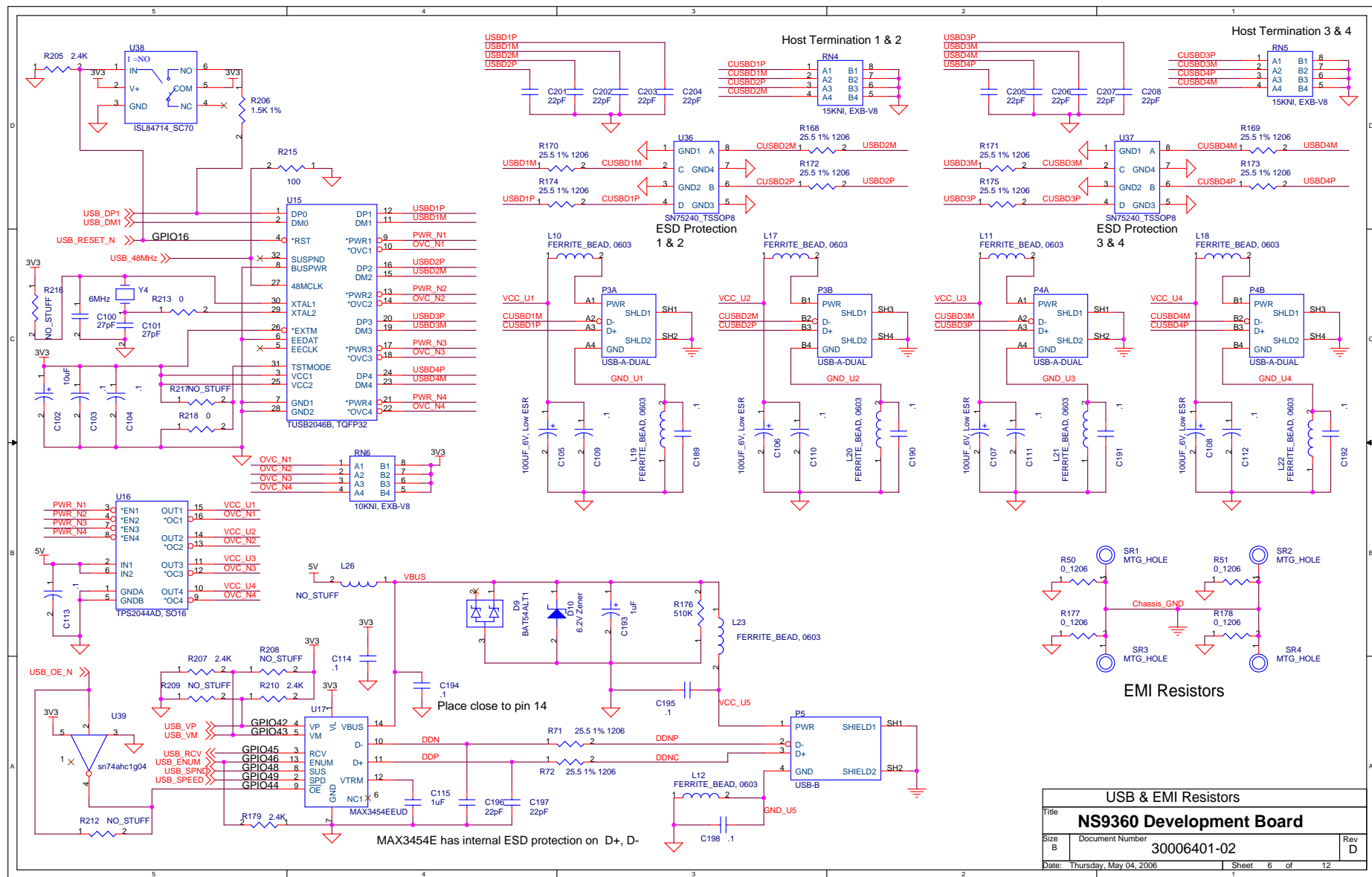
D = Full Debug
P = Production Debug

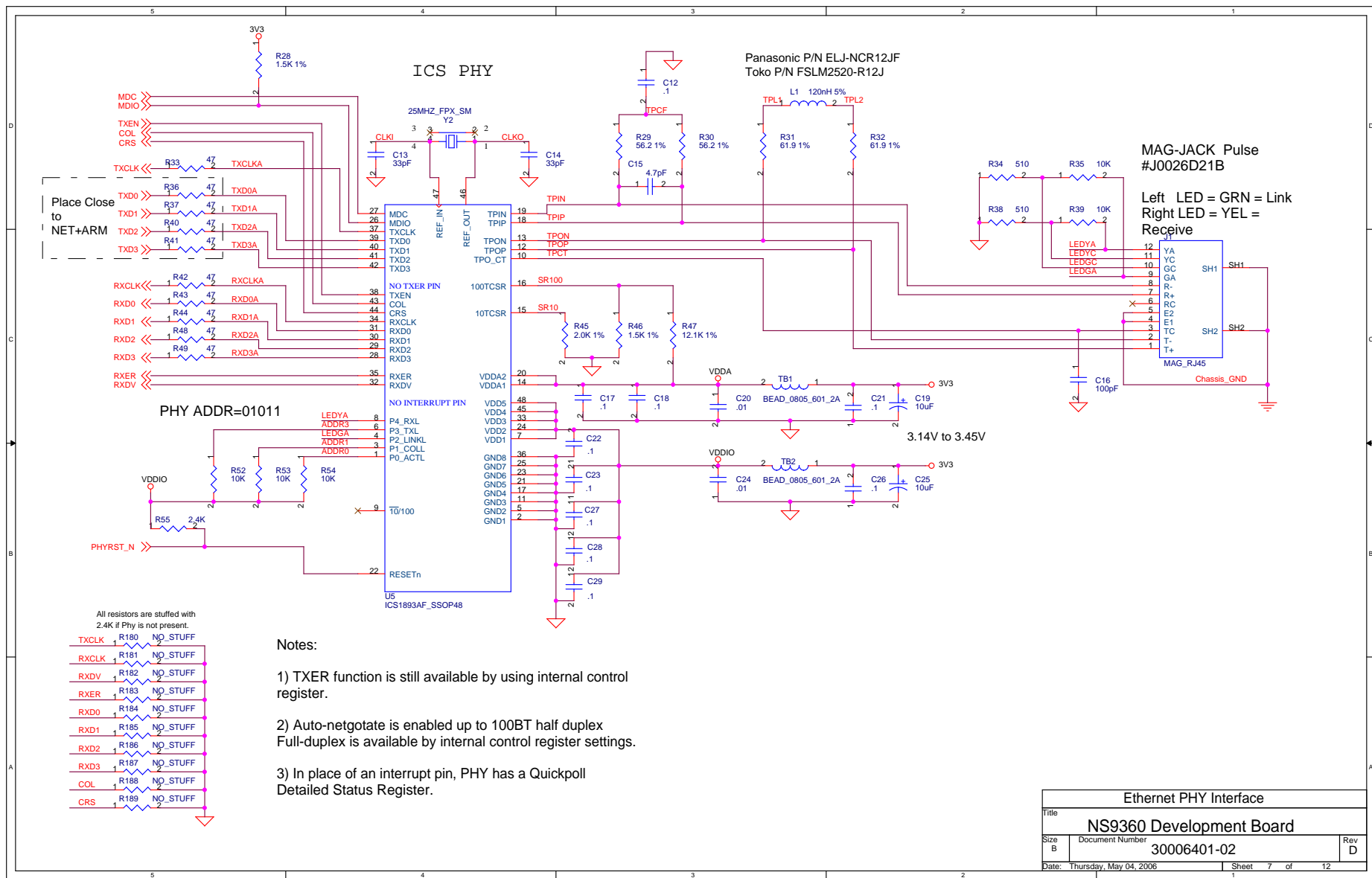
S1 = 4.55V
S2 = 2.93V
S3 = adj(1.25 Ref)

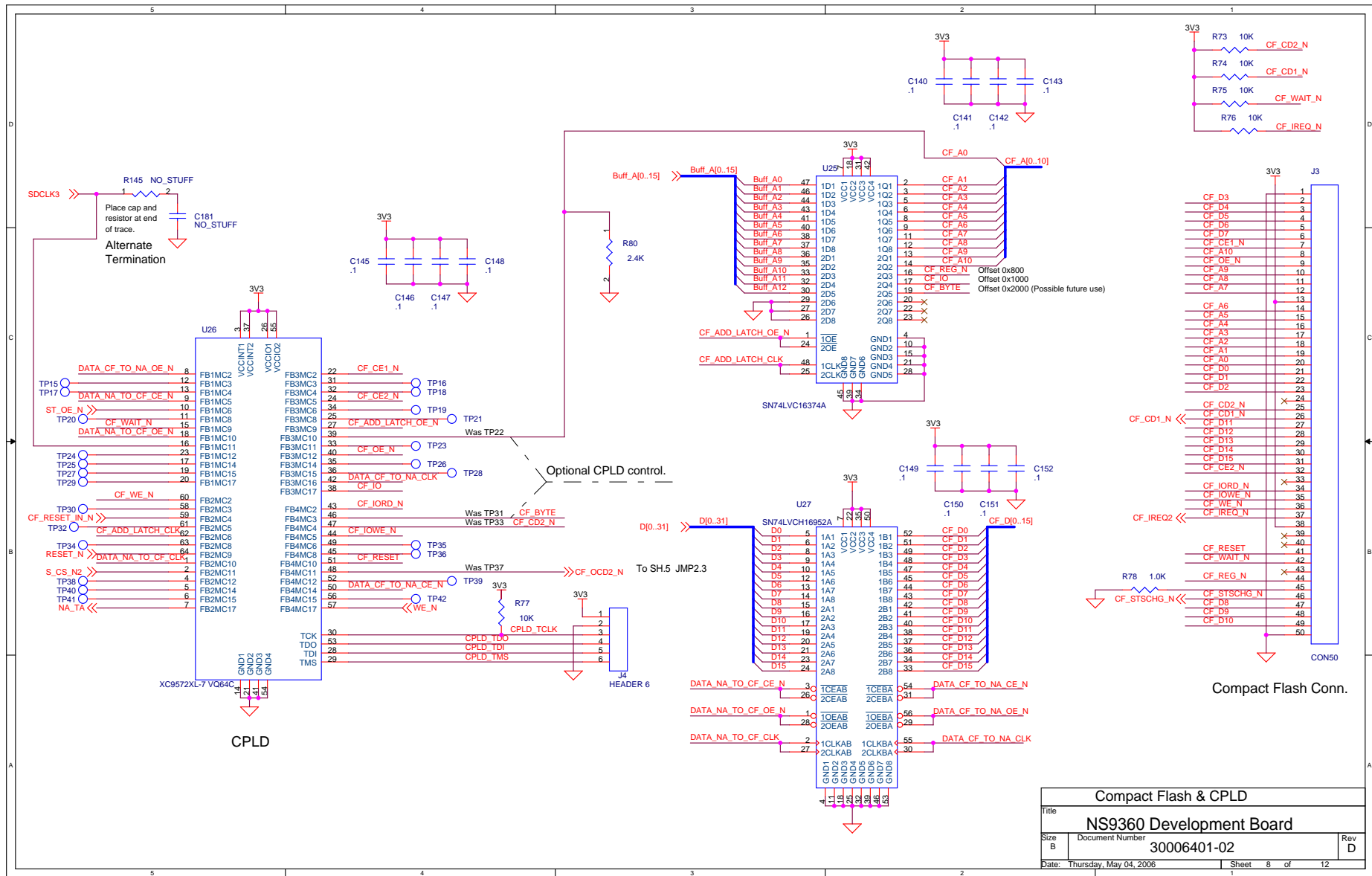




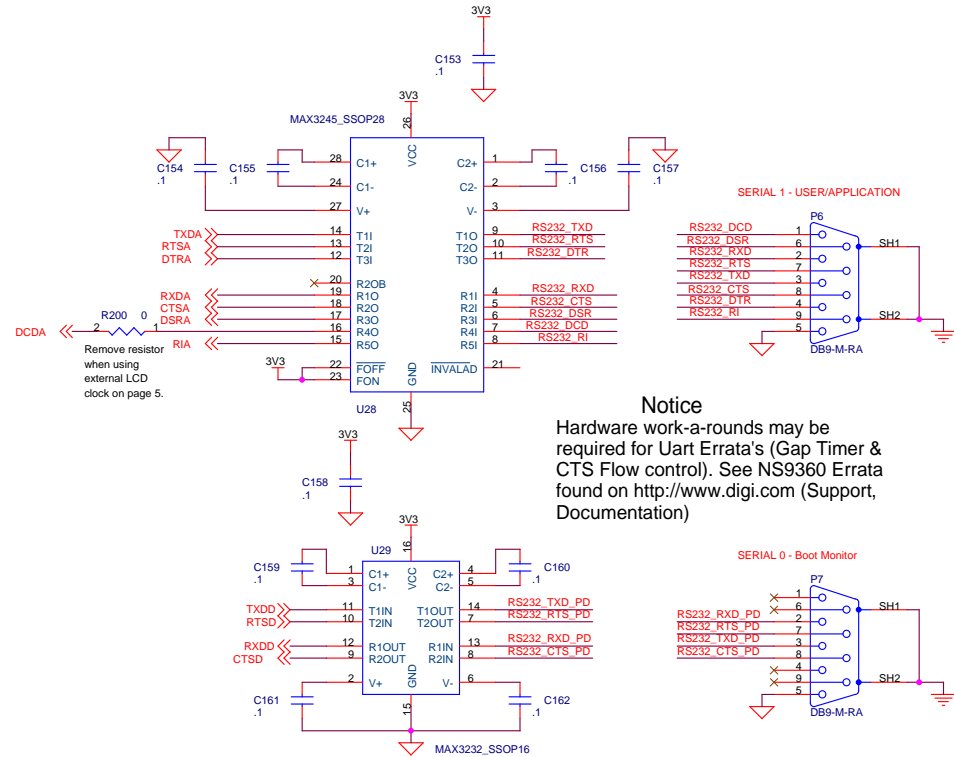




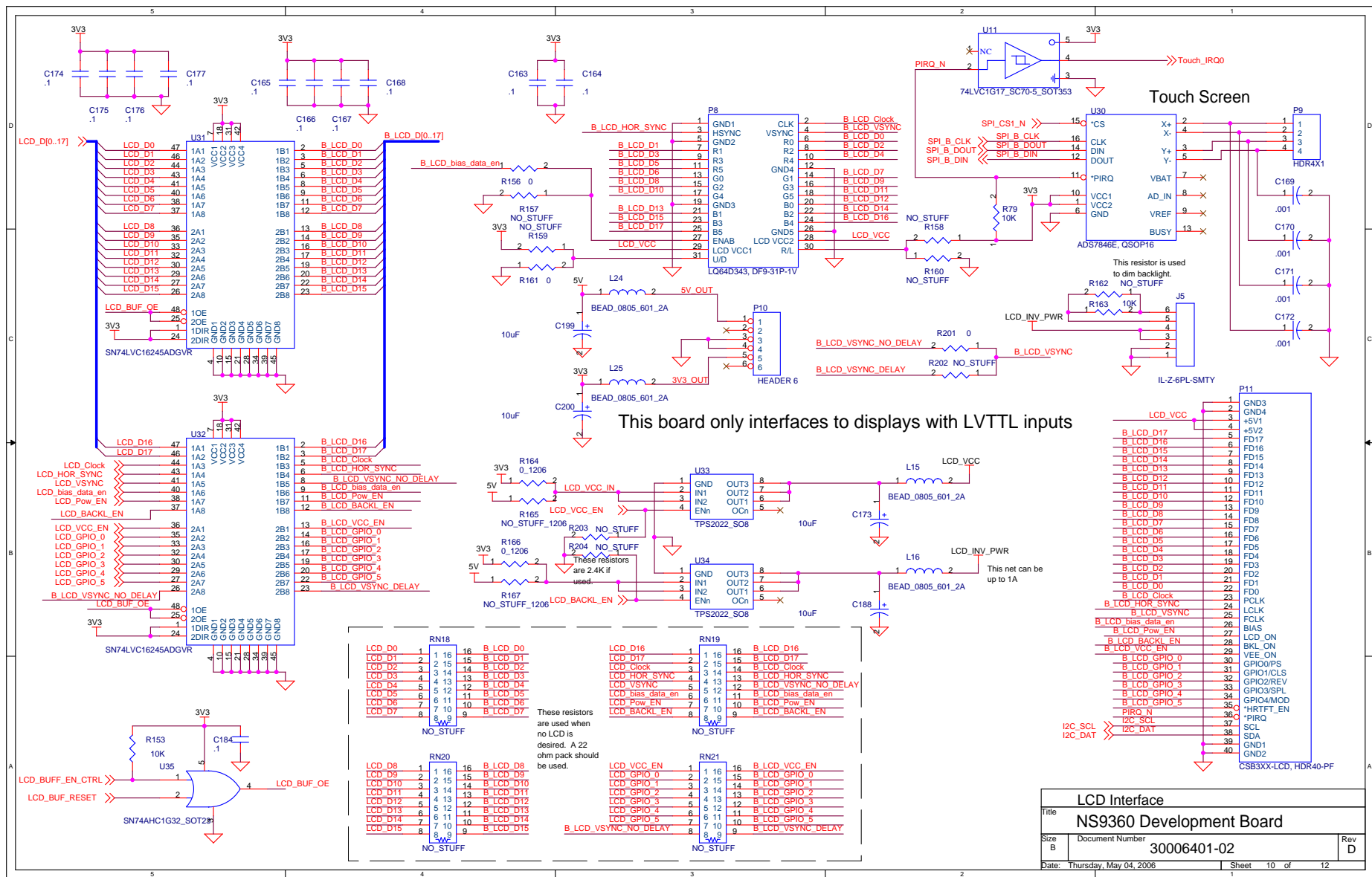


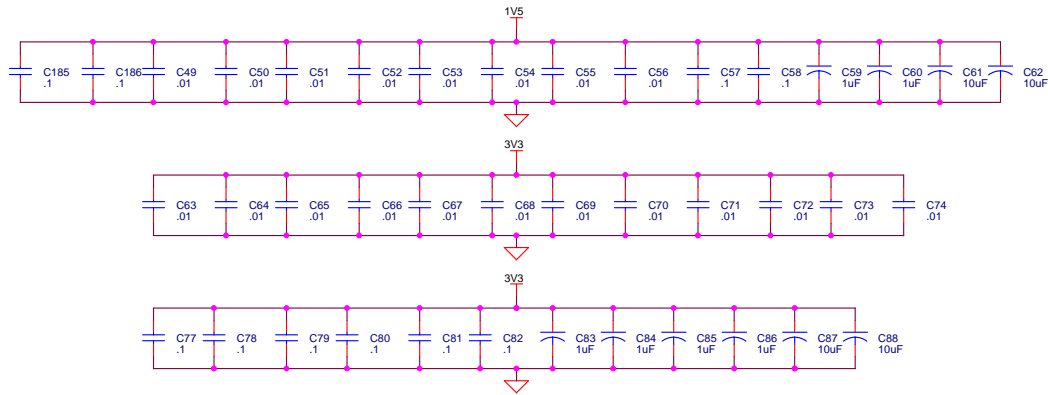
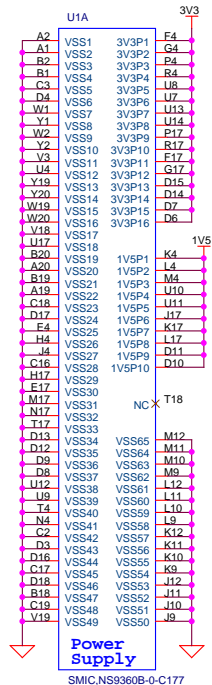


NS9360 Bootstrap Table			
IMPORTANT: All bootstrap inputs have an internal pull-up, and are latched (5) x1_sys_osc clock cycles after reset_n is deasserted (goes high)			
rtkc - byte_lane_sel_n[3:0] Static Chip select 1 rtkc PB S_CS1 mode 1 0 Write Enable 0 1 Byte Lane Enable No pull-down defaults to Write Enable (rtkc into FS is inverted)			
reset_done - Boot Up Mode reset_done BMM Boot Up Mode 0 0 Boot from SPI on Serial port B 1 1 Boot from S_CS1 Flash/ROM No pull-down boots from S_CS1 Flash/ROM			
gpio[2],[0] - PLL FS[1:0] (PLL Frequency Select) gpio FS Divide by 10 00 1 11 01 2 00 10 4 01 11 8 No pull-down defaults to Divide by 2 (gpio[2] into FS is inverted)			
gpio[17],[12],[10],[8],[4] - PLL ND[4:0] (PLL Multiplier, ND+1). Sample clock frequency setting with 29.4912 MHz input clock and FS/2 gpio PLLND ND+1 Frequency (MHz) 10010 10111 24 176.9472 10001 10100 21 154.8288 01000 01101 14 103.2192 gpio[10] and [4] into PLLND are inverted. ND+1 of 24 = 176.9472MHz, pull-down GPIO[12], GPIO[10], GPIO[4] ND+1 of 21 = 154.8288MHz, pull-down GPIO[12], GPIO[10], GPIO[8] ND+1 of 14 = 103.2192MHz, pull-down GPIO[17], GPIO[10], GPIO[8], GPIO[4] Note: No pull-downs = ND+1 of 27. This is out of range for the NS9360.			
gpio[19] - Reserved. gpio PLLBP Mode 0 0 PLL is bypassed 1 1 PLL Not bypassed No pull-down enables the PLL (Should NEVER be pulled down during boot)			
gpio[24],[20] - Static Chip select 1 data width gpio MW Data Width 01 00 8 bits 00 01 16 bits 11 10 32 bits 10 11 Reserved No pull-down defaults to x32 bit Flash/ROM (gpio[20] into MW is inverted)			
gpio[44] - Endian Mode gpio END Mode 1 0 Little endian 0 1 Big endian No pull-down defaults to Little endian (gpio[44] into END is inverted)			
gpio[49] - Static Chip select 1 polarity gpio PC S_CS1 polarity 1 0 Active low 0 1 Active high No pull-down defaults to Active low (gpio[49] into PC is inverted)			



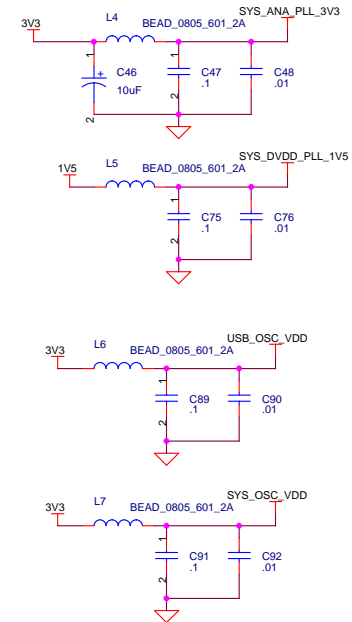
RS232 Outputs & Bootstrap Table			
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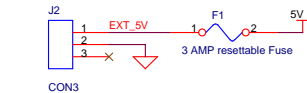


Notice

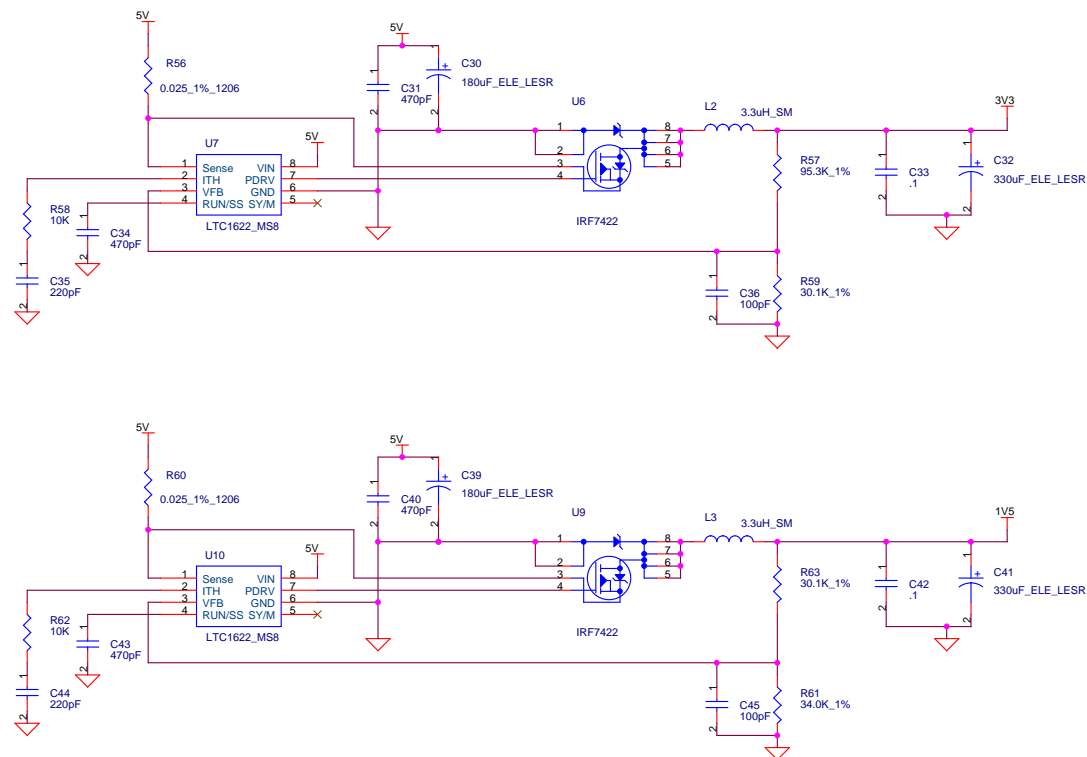
Isolated power planes are recommended for the NS9360 's 3V3 and 1V5 power pins. See NS9360 design rules found on <http://www.digi.com> (Support, Documentation)



NS9360 Power Supply pins and filter caps			
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Center Pin +, 5.5mm



Important Disclaimer:

"This power supply design may not meet the latest, required power supply sequencing. See the NS9360 Hardware Reference Guide or Data Sheet for power sequencing specification, or consult factory for power supply design examples".

Power Supply		
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