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1. History

Date	Version	Responsible	Description
18/02/05	1.0	K Rudolf	Initial Version
07.03.2005	1.1	K Rudolf	Ethernet LEDs need external resistor
10.03.2005	1.2	K Rudolf	Restructuring showing state after U-Boot
23.03.2005	1.3	K Rudolf	Changes due to A9M9750_2

2. Preface

A9M9750 Module is a member of the ARM9 family with CPUs of different manufactorers. It has a NetSilicon NS9750 CPU, a 32-bit machine with up to 200MHz clock speed. The tables in the next sides describe every pin of the 2 X 120 pole connectors of the module, its properties and the usage of it on the A9M9750DEV_1 board.

3. A9M9750 Module Pinning

Legend pin specification in table:

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after UBOOT	Application A9M9750DEV_1
				module specific pins		
				common pins to all A9M modules		

Legend Type:
I: Input
O: Output
I/O: Input or Output
P: Power

Legend RESET state:
PUW: Weak pull up to switched 3.3V in CPU on module
PU10: Pull up 10K to switched 3.3V on module

Legend A9M9750 Name:
GPIO names show GPIO/Function0_UART/Function0_misc/Function1/Function2
GPIOSWX: no connection to GPIOX, when RESET# asserted (is strapping pin)

3.1. Connector X1

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after U-Boot	Application A9M9750DEV_1
1	P	-	-	GND		
2	I	-		RSTIN#	Reset Input allowing manual or remote RESET Pull up 10K to +3.3V on module paralleled by 10..14K internal pull up in RESET controller U16	Connected via 470R to output RES# RESET controller U16 supervising 1.5V, 3.3V and manual RESET push-button on DEV board
3	I/O	-		PWRGOOD	Output of the reset controller push pull with 470R current limiting resistor	Connected as PWRGOOD to Mulit-ICE connector X13 pin 15
4	O	RSTOUT#		RSTOUT#	Output of CPU RESET_DONE logical ANDed with PWRGOOD: High after SPI boot loading finished	Connected as RSTOUT# to FPGA U17 and CPLD U2
5	I	-	PU10	TCK	JTAG	Connected to X12 (JTAG Booster) and X13 (Multi-ICE)
6	I	-	PU10	TMS	JTAG	Connected to X12 (JTAG Booster) and X13 (Multi-ICE)
7	I	-	PU10	TDI	JTAG	Connected to X12 (JTAG Booster) and X13 (Multi-ICE)
8	O	-	PU10	TDO	JTAG	Connected to X12 (JTAG Booster) and X13 (Multi-ICE)
9	I	-	PU10	TRST#	JTAG	Connected to X12 (JTAG Booster) and X13 (Multi-ICE)
10	I	-	PU10	CONF0/ DEBUGEN#	Debug Enable, 0 = Debug enabled, TRST# isolated from SRST#	Connected to DIP-switch S4.1 ON: connected to GND
11	I	-	PU10	CONF1/ NAND_FWP#	NAND Flash Write Protect, 0 = NAND Flash write protected	Connected to DIP-switch S4.2 ON: connected to GND
12	I	-	PU10	CONF2/ OCD_EN#	Enables OCD mode, use with CONF0	Connected to DIP-switch S4.3 ON: connected to GND
13	I	-	PU10	CONF3/ (PCI/CARDBUS#)	PCI or CardBus 0 = CardBus enabled 1 = PCI enabled	Connected to DIP-switch S4.4 ON: connected to GND
14	I/O	I	PU10	CONF4 GPIO38, 2K2 in serie		Connected to DIP-switch S4.5

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after U-Boot	Application A9M9750DEV_1
				Bit28 GEN_ID		ON: connected to GND
15	I/O	I	PU10	CONF5 GPIO38, 2K2 in serie Bit29 GEN_ID		Connected to DIP-switch S4.6 ON: connected to GND
16	I/O	I	PU10	CONF6 GPIO38, 2K2 in serie Bit30 GEN_ID		Connected to DIP-switch S4.7 ON: connected to GND
17	I/O	I	PU10	CONF7 GPIO38, 2K2 in serie Bit31 GEN_ID		Connected to DIP-switch S4.8 ON: connected to GND
18	I/O		PU10	GPIOSW8/ TXDA/ SPIA_DO/ reserved/ reserved	GPIO Input	Connected as SPIA_DO (Output, Funct 0 SPI) to Touch Controller LCD, X27
19	I/O		PUW	GPIO9/ RXDA/ SPIA_DI/ reserved/ timer 8 dupe	GPIO Input	Connected as SPIA_DI (Input, Funct 0 SPI) to Touch Controller LCD, X27
20	I/O		PU10	GPIOSW10 RTSA#/ -/ reserved/ reserved/	GPIO Iinput RTSA# with NS9750B CPU unusable (Bug CPU Prototypes)	Connected as AUD_WS (Output, Funct 3) to Audio chip U6
21	I/O	EIRQ2#	PUW	GPIO11/ CTSA#/ -/ EIRQ2 dupe/ timer 0 dupe	GPIO Input	Connected as EIRQ2 Input, Funct 1) to FPGA U17 and CPLD U2, 10K pull up on DEV board
22	I/O	-	PU10	GPIOSW12/ DTRA#/ -/ reserved/ reserved	GPIO Input	Connected as FPGA_CS0# (Output, Funct 3) via switch U41 to FPGA EEPROM U10
23	I/O	-	PU10	GPIO13/ DSRA# -/ EIRQ0 dupe/ timer 10 dupe	GPIO Input	Connected as EIRQ0 (Input, Funct 1) to RTC_INT# on Module; logical OR with open drain possible
24	I/O	TxDB	PU10	GPIOSW0/ TXDB/ SPIB_DO/ DMA0_DONE dupe/ timer 1 dupe	TXD Console (Output, Funct 0 UART)	Connected as SPIB_DO (Output, Funct 0 SPI) to audio chip U6
25	I/O	RxDB	PUW	GPIO1/ RXDB/ SPIB_DI/ DMA0_REQ dupe/ EIRQ0	RXD Console (Input, Funct 0 UART)	Connected as SPIB_DI (Input, Funct 0 SPI) via R58 to audio chip U6
26	I/O		PU10	GPIOSW2/ RTSB#/ -/ timer 0/ DMA1_ACK/	GPIO Input	Connected as L3_CLK (Output, Funct 3) to audio chip U6
27	I/O		PUW	GPIO3/ CTSB#/ -/ 1284_ACK#/ DMA0_REQ#	GPIO Input	Connected as DMA0_REQ# (Input, Funct 2) to FPGA U17 and CPLD U2
28	I/O	-	PU10	GPIOSW4/ DTRB#/ -/ 12284P_BUSY/ DMA0_DONE	GPIO Input	Connected as L3MODE (Output, Funct 3) to audio chip U6
29	I/O	-	PUW	GPIO5/ DSRB#/ -/ 1284P_ERR/ DMA0_ACK	GPIO Input	Connected as DMA0_ACK (Output, Funct 2) to FPGA U17 and CPLD U2
30	I/O	-	PUW	GPIO6/ RIB#	GPIO Input	Connected as SPIB_CLK (Funct 0 SPI) to audio chip

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after U-Boot	Application A9M9750DEV_1
				/SPIB_CLK/ 1284P_FAULT#/ DMA0_ACK		U6 and FPGA U17
31	I/O	-	PUW	GPIO7/ DCDB#/ SPIB_EN#/ DMA0_ACK dupe/ EIRQ1	GPIO Input	Connected as SPIB_EN# (Funct 0 SPI) to FPGA U17
32	I	-	PUW	WAIT#	external WAIT# input	Connected as WAIT# to FPGA U17 and CPLD U2
33	O	-	-	A24	ext Address	Connected as A24 to FPGA U17
34	O	-	-	A25	ext Address	Connected as A25 to FPGA U17
35	O	-	-	A26	ext Address	accessible at X11 C9
36	O	-	-	A27	ext Address	accessible at X11 D9
37	I/O	I/O	PU10	GPIOSW24/ DTRD#/ -/ LCDD0/ reserved	LCD Data	Connected as LCDD0 (I/O, Funct 1) to X25
38	I/O	I/O	PUW	GPIO25/ DSRD#/ -/ LCDD1 timer 15 dupe	LCD Data	Connected as LCDD1 (I/O, Funct 1) to X25
39	P	P	-	GND		
40	I/O	I/O	PUW	GPIO26/ RID#/ SPID_CK/ LCDD2/ timer 3	LCD Data	Connected as LCDD2 (I/O, Funct 1) to X25
41	I/O	I/O	PUW	GPIO27/ DCDD#/ SPID_EN#/ LCDD3/ timer 4	LCD Data	Connected as LCDD3 (I/O, Funct 1) to X25
42	I/O	I/O	PUW	GPIO28/ -/ EIRQ1 dupe/ LCDD4/ LCDD8 dupe	LCD Data	Connected as LCDD4 (I/O, Funct 1) to X25
43	I/O	I/O	PUW	GPIO29/ -/ timer 5/ LCDD5/ LCDD9 dupe	LCD Data	Connected as LCDD5 (I/O, Funct 1) to X25
44	I/O	I/O	PUW	GPIO30/ -/ timer 6/ LCDD6/ LCDD10 dupe	LCD Data	Connected as LCDD6 (I/O, Funct 1) to X25
45	I/O	I/O	PUW	GPIO31/ -/ timer 7/ LCDD7 LCDD11 dupe	LCD Data	Connected as LCDD7 (I/O, Funct 1) to X25
46	I/O	I/O	PUW	GPIO32/ -/ EIRQ2/ 1284_D0/ LCDD8	LCD Data	Connected as LCDD8 (I/O, Funct 1) to X25
47	I/O	I/O	PUW	GPIO33/ -/ timer 8/ 1284_D1/ LCDD9	LCD Data	Connected as LCDD9 (I/O, Funct 1) to X25
48	I/O	I/O	PUW	GPIO34/ -/ timer 9/ 1284_D2/ LCDD10	LCD Data	Connected as LCDD10 (I/O, Funct 1) to X25

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after U-Boot	Application A9M9750DEV_1
49	I/O	I/O	PUW	GPIO35/ -/ TIMER 10/ 1284_D3/ LCDD11	LCD Data	Connected as LCDD11 (I/O, Funct 1) to X25
50	I/O	I/O	PUW	GPIOSW36/ -/ reserved/ 1284_D4/ LCDD12	LCD Data	Connected as LCDD12 (I/O, Funct 1) to X25
51	I/O	I/O	PUW	GPIOSW37/ -/ reserved/ 1284_D5/ LCDD13	LCD Data	Connected as LCDD13 (I/O, Funct 1) to X25
52	I/O	I/O	PU10	GPIOSW38/ -/ reserved/ 1284_D6/ LCDD14	LCD Data	Connected as LCDD14 (I/O, Funct 1) to X25
53	I/O	I/O	PU10	GPIOSW39/ -/ reserved/ 1284_D7/ LCDD15	LCD Data	Connected as LCDD15 (I/O, Funct 1) to X25
54	I/O	I/O	PU10	GPIOSW40/ TXDC/ SPIC_DO/ EIRQ3/ LCDD16	LCD Data	Connected as LCDD16 (I/O, Funct 1) to X25
55	I/O	I/O	PU10	GPIOSW41/ RXDC/ SPIC_DI/ timer 11/ LCDD17	LCD Data	Connected as LCDD17 (I/O, Funct 1) to X25
56	I/O	-	PUW	GPIO42/ RTSC#/ -/ timer 12/ LCDD18	GPIO Input	Connected as FPGA_DCLK (Output, Funct 3) via switch U41 to FPGA EEPROM U10
57	I/O	-	PUW	GPIO43/ CTSC#/ -/ timer 13/ LCDD19	GPIO Input	Connected as FPGA_DATA0 (Input, Funct3) via switch U41 to FPGA EEPROM U10
58	I/O	-	PU10	GPIOSW44/ TXDD/ SPID_DO/ 1284_SEL LCDD20	GPIO Input	Connected as FPGA_ASD0 (Output, Funct 3) via switch U41 to FPGA EEPROM U10
59	I/O	-	PUW	GPIO45/ RXDD/ SPID_DI/ 1284_STB#/ LCDD21	GPIO Input	Connected GPIO45(Input, Funct 3) to U1 (user key 1)
60	I/O	-	PUW	GPIO46/ RTSD#/ -/ 1284_AFD# LCDD22	GPIO Input RTSD# unusable with NS9750B CPUs (Bug prototype modules)	Connected as GPIO46 (Input, Funct 3) to U2 (user key 2)
61	I/O	-	PUW	GPIO47/ CTSD#/ -/ 1284_INIT#/ LCDD23	GPIO Output	Connected as GPIO47 (Output, Funct3) via J13 to LE4 (Debug LED)
62	O		PUW	GPIO18/ -/ ECAM_REJ/ LCD_PWREN#/ EIRQ3 dupe	LCD Control	Connected as LCD_PWREN# (Output, Funct 1 or Funct 3) to X25
63	O		PUW	GPIO22/ RIC#/	LCD Control	Connected as LCD_AC_BDE (Output, Funct 1) to X25

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after U-Boot	Application A9M9750DEV_1
				SPIC_CK/ LCD_AC_BDE/ reserved		
64	O		PUW	GPIO21/ DSRC#/ -/ LCD_VFRAME reserved	LCD Control	Connected as LCD_VFRAME (Output, Funct 1) to X25
65	O		PU10	GPIOSW19/ -/ ECAM_REQ/ LCD_HSYNC/ DMA1_ACK#	LCD Control	Connected as LCD_HSYNC (Output, Funct 1) to X25
66	O		PU10	GPIOSW20/ DTRC#/ -/ LCD_CLK/ reserved	LCD Control	Connected as LCD_CLK (Output, Funct 1) to X25
67	O		PUW	GPIO23/ DCDC#/ SPIC_EN#/ LCD_LEND timer 14 dupe	LCD Control	Connected as LCD_LEND (Output, Funct 1) to X25
68	O	-		A0	external address	Connected to FPGA U17 and CPLD U2
69	O	-		A1	external address	Connected to FPGA U17 and CPLD U2
70	O	-		A2	external address	Connected to FPGA U17 and CPLD U2
71	O	-		A3	external address	Connected to FPGA U17 and CPLD U2
72	O	-		A4	external address	Connected to FPGA U17 and CPLD U2
73	O	-		A5	external address	Connected to FPGA U17 and CPLD U2
74	O	-		A6	external address	Connected to FPGA U17 and CPLD U2
75	O	-		A7	external address	Connected to FPGA U17 and CPLD U2
76	O	-		A8	external address	Connected to FPGA U17
77	O	-		A9	external address	Connected to FPGA U17
78	O	-		A10	external address	Connected to FPGA U17
79	P	-	-	GND		
80	O	-		A11	external address	Connected to FPGA U17
81	O	-		A12	external address	Connected to FPGA U17
82	O	-		A13	external address	Connected to FPGA U17
83	O	-		A14	external address	Connected to FPGA U17
84	O	-		A15	external address	Connected to FPGA U17
85	O	-		A16	external address	Connected to FPGA U17
86	O	-		A17	external address	Connected to FPGA U17
87	O	-		A18	external address	Connected to FPGA U17
88	O	-		A19	external address	Connected to FPGA U17
89	O	-		A20	external address	Connected to FPGA U17
90	O	-		A21	external address	Connected to FPGA U17
91	O	-		A22	external address	Connected to FPGA U17
92	O	-		EXT_OE#		Connected to FPGA U17and CPLD U2
93	O	-		EXT_WE#	22R series resistor on module	Connected to FPGA U17 and CPLD U2
94	O	-		A23	external address	Connected to FPGA U17
95	O	CS0#		CS0#	Chip select, not used on module, Defaults to Ouput/High at reset.	Connected to FPGA U17 and CPLD U2
96	O	CS2#		CS2#	Chip select, not used on module, Defaults to Ouput/High at reset.	Connected to FPGA U17 and CPLD U2
97	O	CS3#		CS3#	Chip select, not used on module, Defaults to Ouput/High at reset.	Connected to FPGA U17 and CPLD U2
98	-	-	-	NC	-	
99	O	-	-	PWREN	power sequencing control (n.a. at A9M9750_0 prototypes)	switches +3.3V on board
100	-	-	-	NC (reserved as	-	

X1	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description after U-Boot	Application A9M9750DEV_1
				BATT_FLT#)		
101	I/O	-	PUW	GPIO48/ -/ timer 14/ 1284_SELIN#/ DMA1_REQ#	GPIO Input	unused
102	I/O	-	PUW	GPIO16 -/ reserved/ 1284_JAM# dupe/ timer 11 dupe	GPIO Input	Connected as USB_OVRCURR (Input, Funct 3) to U8
103	O	-	No	EXT_BE0#	Upper Byte/Lower Byte Enable	Connected as EXT_BE0# to FPGA U17
104	O	-	No	EXT_BE1#	Upper Byte/Lower Byte Enable	Connected as EXT_BE1# to FPGA U17
105	O	-	No	EXT_BE2#	Upper Byte/Lower Byte Enable	Connected as EXT_BE2# to FPGA U17
106	O	-	No	EXT_BE3#	Upper Byte/Lower Byte Enable	Connected as EXT_BE3# to FPGA U17
107	I/O	-	PUW	GPIO15 DCDA#/ SPIA_EN#/ timer 2/ reserved	GPIO, Input	Connected as SPIA_EN# (Output, Funct 3) to X27 (touch LCD)
108	-	-	-	NC	-	
109	-	-	-	NC	-	
110	I/O		PUW	GPIO14 RIA#/ SPIA_CLK/ Timer 1/ Reserved	GPIO Input	Connected as SPIA_CLK (Output, Funct 0 SPI) to X27
111	O	IICSCL		IICSCL	I²C clock, Pullup 4k7 to 3.3V on module	
112	I/O	IICSDA		IICSDA	I²C data, Pullup 4k7 to 3.3V on module	
113	I/O	I	PU10	GPIOSW17/ -/ USB_PWR/ reserved/ reserved	GPIO Input	Connected as USB_ENUM# (Output, funct 3) for USB device 3 to switch on 1k5 pull-up resistor
114	I/O	USBP	No	USB_INTPHY_P	USB host/device	USB data line +, connected via R95 to expansion connector X10
115	I/O	USBN	No	USB_INTPHY_N	USB host/device	USB data line -, connected via R96 to expansion connector X1
116	P	-	-	VRTC	Backup Battery for RTC, for 3V cell, power-switch-over is on the module, Can be left floating, if RTC backup not needed.	3V battery connected
117	P	-	-	GND		
118	P	-	-	3.3V_IN	unswitched 3.3V	3.3V to module
119	P	-	-	VLIO	Mobile: Power from Li-Ion Battery Non-Mobile: connected to 3.3V	Delivers either power from Li-Ion battery or 3.3V_IN
120	P	-	-	3.3V_IN	unswitched 3.3V	3.3V to module

3.2. Connector X2

X2	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description	Application A9M9750/A9M9360DEV_1
1	I/O	-	PU10	PCI_INTA#		Connected to X28
2	P	-		GND		
3	I	-	PU10	PCI_INTC#		
4	I/O	-	PU10	PCI_INTB#		
5	O	-		PCI_RESET#		Connected to FPGA U17 for PCI patch
6	I	-	PU10	PCI_INTD#		
7	O	-	PU10	PCI_GNT0#	Connected via R43 to PCI_GNT1#	
8	P	-		GND		
9	O	-	PU10	PCI_GNT1#		Connected to X28
10	O	-		PCI_CLKOUT		Not used
11	I	-	PUW	PCI_CLKIN		Connected to PCI_CLK_MOD
12	O	-	PU10	PCI_GNT2#		
13	O	-	PU10	PCI_GNT3#		
14	P	-		GND		
15	I/O	-		PCI_AD30		Connected to X28
16	I	-		PCI_REQ0#	Connected via R44 to PCI_REQ1#	
17	I	-	PU10	PCI_REQ1#		Connected to FPGA U17 for PCI arbiter patch; MPCI_REQ1# on X28 via R140 to unpatched PCI_REQ1# to module
18	I	-	PU10	PCI_REQ2#		
19	I	-	PU10	PCI_REQ3#		
20	I/O	-		PCI_AD31		Connected to X28
21	I/O	-		PCI_AD28		Connected to X28
22	I/O	-		PCI_AD29		Connected to X28
23	I/O	-		PCI_AD26		Connected to X28
24	I/O	-		PCI_AD27		Connected to X28
25	I/O	-		PCI_AD24		Connected to X28
26	I/O	-		PCI_AD25		Connected to X28
27	I	-		PCI_IDSEL		Connected to X28, via R92 to PCI_AD16
28	I/O	-		PCI_CBE3#		Connected to X28
29	I/O	-		PCI_AD22		Connected to X28
30	I/O	-		PCI_AD23		Connected to X28
31	I/O	-		PCI_AD20		Connected to X28
32	I/O	-		PCI_AD21		Connected to X28
33	I/O	-		PCI_AD18		Connected to X28
34	I/O	-		PCI_AD19		Connected to X28
35	I/O	-		PCI_AD16		Connected to X28
36	I/O	-		PCI_AD17		Connected to X28
37	I/O	-	PU10	PCI_FRAME#		Connected to X28
38	I/O	-		PCI_CBE2#		Connected to X28
39	I/O	-	PU10	PCI_TRDY#		Connected to X28
40	P	-		GND		
41	I/O	-	PU10	PCI_IRDY#		Connected to X28
42	I/O	-	PU10	PCI_STOP#		Connected to X28
43	I/O	-		PCI_PAR		Connected to X28
44	I/O	-	PU10	PCI_DEVSEL#		Connected to X28
45	I/O	-		PCI_AD15		Connected to X28
46	I/O	-	PU10	PCI_PERR#		Connected to X28
47	I/O	-		PCI_AD13		Connected to X28
48	I/O	-	PU10	PCI_SERR#		Connected to X28
49	I/O	-		PCI_AD11		Connected to X28
50	I/O	-		PCI_CBE1#		Connected to X28
51	I/O	-		PCI_AD9		Connected to X28
52	I/O	-		PCI_AD14		Connected to X28
53	I/O	-		PCI_CBE0#		Connected to X28
54	I/O	-		PCI_AD12		Connected to X28
55	I/O	-		PCI_AD6		Connected to X28
56	I/O	-		PCI_AD10		Connected to X28
57	I/O	-		PCI_AD4		Connected to X28

X2	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description	Application A9M9750/A9M9360DEV_1
58	I/O	-		PCI_AD8		Connected to X28
59	I/O	-		PCI_AD2		Connected to X28
60	I/O	-		PCI_AD7		Connected to X28
61	I/O	-		PCI_AD5		Connected to X28
62	I/O	-		PCI_AD3		Connected to X28
63	I/O	-		PCI_AD1		Connected to X28
64	I/O	-		PCI_AD0		Connected to X28
65	I	-	PUW	LCD_CLKIN		
66	I	-		ETH_TPIN	Ethernet Input-, 100R differential termination on module	Connected via R97 to expansion connector X20
67	O	-		ETH_LEDLNK	Ethernet Line/Activity LED High, when link ok Low, while active.	Connected to Link/Activity LED in RJ45 X17
68	I	-		ETH_TPIP	Ethernet Input+, 100R differential termination on module	Connected via R103 to expansion connector X21
69	O	-		ETH_LEDH	Ethernet High Speed LED High, when 100MB Low, when 10MB	Connected to Speed LED in RJ45 X17
70	O	-		ETH_TPON	Ethernet Output-, 100R differential termination on module	Connected via R98 to expansion connector X20
71	I	-		ETH_ESD0	Connected via 0R to Gnd on module	not used
72	O	-		ETH_TPOP	Ethernet 0 Output+, 100R differential termination on module	Connected via R104 to expansion connector X21
73	P	-		NC (reserved for ETH_EREF)		
74	-	-		NC	R/B#, SmartMedia not supported in future, do not connect	
75	-	-		NC	FWE#, SmartMedia not supported in future, do not connect	
76	-	-		NC	FWE#, SmartMedia not supported in future, do not connect	
77	-	-		NC	FCEEXT#, SmartMedia not supported in future, do not connect	
78	-	-		NC	ALE, SmartMedia not supported in future, do not connect	
79	-	-		NC	CLE, SmartMedia not supported in future, do not connect	
80	P	-		GND		
81	I/O	-		D0	Data Bus	Connected to FPGA U17 and CPLD U2
82	I/O	-		D1		Connected to FPGA U17 and CPLD U2
83	I/O	-		D2		Connected to FPGA U17 and CPLD U2
84	I/O	-		D3		Connected to FPGA U17 and CPLD U2
85	I/O	-		D4		Connected to FPGA U17 and CPLD U2
86	I/O	-		D5		Connected to FPGA U17 and CPLD U2
87	I/O	-		D6		Connected to FPGA U17 and CPLD U2
88	I/O	-		D7		Connected to FPGA U17 and CPLD U2
89	I/O	-		D8		Connected to FPGA U17
90	I/O	-		D9		Connected to FPGA U17
91	I/O	-		D10		Connected to FPGA U17
92	I/O	-		D11		Connected to FPGA U17
93	I/O	-		D12		Connected to FPGA U17
94	I/O	-		D13		Connected to FPGA U17
95	I/O	-		D14		Connected to FPGA U17
96	I/O	-		D15		Connected to FPGA U17
97	I/O	-		D16		Connected to FPGA U17
98	I/O	-		D17		Connected to FPGA U17
99	I/O	-		D18		Connected to FPGA U17
100	I/O	-		D19		Connected to FPGA U17
101	I/O	-		D20		Connected to FPGA U17
102	I/O	-		D21		Connected to FPGA U17
103	I/O	-		D22		Connected to FPGA U17

X2	Type	U-Boot	RESET State	A9M9750 Name	A9M9750 Description	Application A9M9750/A9M9360DEV_1
104	I/O	-		D23		Connected to FPGA U17
105	I/O	-		D24		Connected to FPGA U17
106	I/O	-		D25		Connected to FPGA U17
107	I/O	-		D26		Connected to FPGA U17
108	I/O	-		D27		Connected to FPGA U17
109	I/O	-		D28		Connected to FPGA U17
110	I/O	-		D29		Connected to FPGA U17
111	I/O	-		D30		Connected to FPGA U17
112	I/O	-		D31		Connected to FPGA U17
113	-	-		NC (reserved for A28)		
114	-	-		NC (reserved for A29)		
115	-	-		NC (reserved for A30)		
116	-	-		NC (reserved for A31)		
117	-	-		NC (reserved for CANTXD/CANH)		
118	-	-		NC (reserved for CANRXD/CANL)		
119	O	CLKOUT		BCLKOUT	Clock output, buffered CLKOUT signal	Connected toFPGA U17
120	P	-		GND		