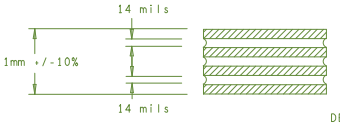
NOTES (UNLESS OTHERWISE SPECIFIED):

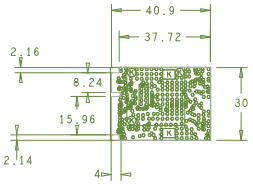
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	XX-XX-11	X.X.



DETAIL A
LAYER STACKUP
SCALE: NONE

		FINISHED Cu WEIGHT
LAYER 1	COMPONENT SIDE	1/2 oz.
LAYER 2	GROUND PLANE	1/2 oz.
LAYER 3	POWER PLANE	1/2 oz.
LAYER 4	SOLDER SIDE	1/2 oz.

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .00X"/.00X"
7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
16. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)
17. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
18. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.
19. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILLIMETERS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
○	0.3048	+0.0762/-0.0762	PLATED	349
ⓧ	2.5908	+0.0508/-0.0508	PLATED	3
⊕	0.6604	+0.1016/-0.0	NON-PLATED	2
K	2.5908	+0.1016/-0.1016	NON-PLATED	2

___ PUBI (PUBLIC INFORMATION)
X FIVO (FREESCALE INTERNAL USE ONLY)
___ FCP (FREESCALE CONFIDENTIAL PROPRIETARY)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MM
TOLERANCES ARE:
DECIMALS ANGLES
XX .01 .5°
XXX .005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDIMENSIONED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN XXXXX	XX-XX-11
CHECKED XXXXX	XX-XX-11
DESIGN ENGINEER XXXXX	XX-XX-11

PART NO. 170-XXXXX

FREESCALE SEMICONDUCTOR
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PAN1326-Silex mini PCIe XXXXX

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-XXXXX	FAB-XXXXX	A

SCALE | DO NOT SCALE DRAWING | SHEET OF