NS9775 / NS9750 / NS9750B-A1 / NS9360
Reset Issue Change Notice

The SDRAM clock enable configuration for the NS9775, NS9750, NS9750B-A1 and NS9360 (NS9xxx) must be changed in order to prevent SDRAM devices from locking up during a manual or brown out condition reset following the initial power on reset. The only exception is if power is cycled automatically during a brown out condition reset and a manual push button reset is not used or if clock enables to the SDRAM devices are connected directly to 3.3V. Otherwise, the SDRAM devices can become locked up during a manual or brown out condition reset as follows:

1. A manual or brown out condition reset is applied to reset_n on the NS9xxx.
2. At the same time, a read command is active to the SDRAM devices connected to the NS9xxx.
3. The reset_n to the NS9xxx shuts off clocks and clock enables to SDRAM devices, preventing the read command from being completed.
4. The SDRAM devices become permanently locked up at this time. A power cycle is required to return the SDRAM devices to normal operation.

NS9775 / NS9750 / NS9750B-A1 Work Around

There are two options to avoid the SDRAM lock up condition during a manual or brown out condition reset on a board using the NS9775, NS9750 or NS9750B-A1:

1. Connect the clock enables on the SDRAM devices directly to 3.3V or pull-up resistor.
2. Use a switch to connect clock enables to the SDRAM devices to a pull-up resistor until the NS97xx device reset is complete as indicated by a high level on the reset_done output. A sample circuit is shown in Figure 1 below.

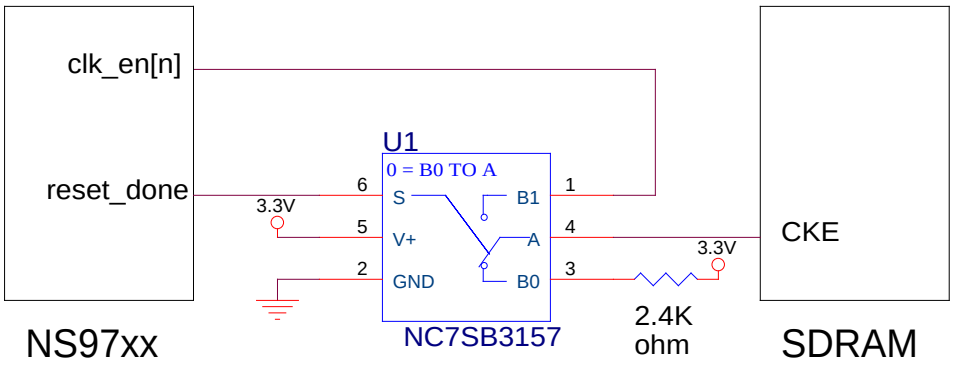

Figure 1: NS97xx Clock Enable Configuration

NS9360 Work Around

There are two options to avoid the SDRAM lock up condition during a manual or brown out condition reset on a board using the NS9360:

3. Connect the clock enables on the SDRAM devices directly to 3.3V or pull-up resistor.
4. Connect a 10-15k pull up resistor on the clock enable signals between the NS9360 and the SDRAM devices.