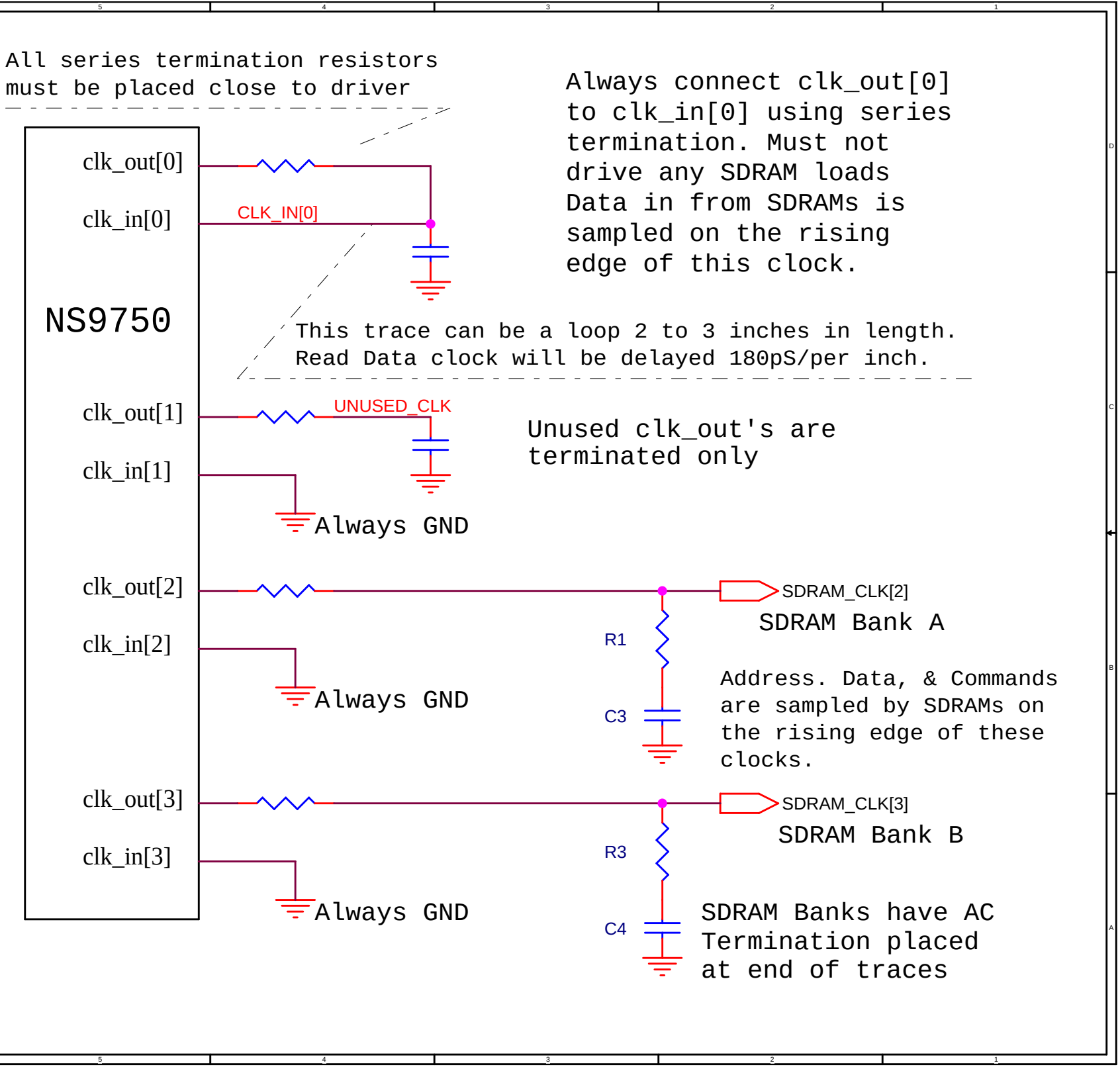
All series termination resistors must be placed close to driver
Always connect clk_out[0] to clk_in[0] using series termination. Must not drive any SDRAM loads Data in from SDRAMs is sampled on the rising edge of this clock.
clk_out[0]
clk_in[0]
CLK_IN[0]
NS9750
This trace can be a loop 2 to 3 inches in length.
Read Data clock will be delayed 180pS/per inch.
clk_out[1]
UNUSED_CLK
clk_in[1]
Unused clk_out's are terminated only
Always GND
clk_out[2]
clk_in[2]
SDRAM_CLK[2]
SDRAM Bank A
R1
C3
Always GND
Address. Data, & Commands are sampled by SDRAMs on the rising edge of these clocks.
clk_out[3]
clk_in[3]
SDRAM_CLK[3]
SDRAM Bank B
R3
C4
Always GND
SDRAM Banks have AC Termination placed at end of traces