There are 73 I/O pins that are shared by the low speed peripheral modules. Each I/O is 4:1 muxed as shown in the spreadsheet.

Port Number	Select 0 Signal Name	Select 1 Signal Name	Select 2 Signal Name	Select 3 Signal Name	Select 0 Description	Select 1 Description	Select 2 Description	Select 3 Description	mA
0 (HW strap)	TxDB (O)	DONE0 (O)	TIMER1 (I/O)	PORT0 (I/O)	ser port B TxData / SPI port B dout	DMA channel 0 Done - duplicate	Timer1 I/O-duplicat	GPIO0	2
1	RxDB (I)	DREQ0 (I)	EIRQ0 (I)	PORT1 (I/O)	ser port B RxData / SPI port B din	DMA channel 0 Req - duplicate	Ext IRQ 0	GPIO1	2
2 (HW strap)	RTSB_ (O)	TIMER0 (I/O)	DACK1 (O)	PORT2	ser port B RTS	Timer0 I/O	DMA channel 1 Ack	GPIO2	2
3	CTSB_ (I)	PACK_ (O)	DREQ0 (I)	PORT3	ser port B CTS	1284 periph ack	DMA channel 0 Req	GPIO3	2
4 (HW strap)	DTRB_ (O)	PBUSY (O)	DONE0 (O)	PORT4	ser port B DTR	1284 periph busy	DMA channel 0 Done	GPIO4	2
5	DSRB_ (I)	PERR (O)	DACK0 (O)	PORT5 (I/O)	ser port B DSR	1284 periph error	DMA channel 0 Ack	GPIO5	2
6	RxCB (I/O) / RIB_ (I) / SPIB_CK(I/O)	PFLT_ (O)	TIMER7 (I)	PORT6 (I/O)	ser port B RxClk / ser port B RI / SPI port B Clk	1284 paper out/jam	Timer7 I/O-dupliat	GPIO6	2
7	TxCB (I/O) / DCDB_ (I) / SPIB_EN(I/O)	DACK0 (O)	EIRQ1 (I)	PORT7 (I/O)	ser port B TxClk / ser port B DCD / SPI port B enable	DMA channel 0 Ack - duplicate	Ext IRQ 1	GPIO7	2
8 (HW strap)	TxDA (O)			PORT8 (I/O)	ser port A TxData / SPI port A dout			GPIO8	2
9	RxDA (I)			PORT9 (I/O)	ser port A RxData / SPI port A din			GPIO9	2
10 (HW strap)	RTSA_ (O)		PWM_0 (O)	PORT10 (I/O)	ser port A RTS		PWM_0 duplicat	GPIO10	2
11	CTSA_ (I)	EIRQ2 (I)	TIMER0 (I/O)	PORT11	ser port A CTS	Ext IRQ 2	Timer0 I/O-	GPIO11	2
12 (HW strap)	DTRA_ (O)		PWM_1 (O)	PORT12 (I/O)	ser port A DTR		PWM_1 duplicat	GPIO12	2
13	DSRA_ (I)	EIRQ0 (I)	PWM_2 (O)	PORT13	ser port A DSR	Ext IRQ0-duplicat	PWM_2 duplicat	GPIO13	2
14	RxCA (I/O) / RIA_ (I) / SPIA_CK(I/O)	TIMER1 (I/O)	PWM_3 (O)	PORT14 (I/O)	ser port A RxClk / ser port A RI / SPI port A Clk	Timer1 I/O	PWM_3 duplicat	GPIO14	2
15	TxCA (I/O) / DCDA_ (I) / SPIA_EN(I/O)	TIMER2 (I/O)	lcd_clk_in (I)	PORT15 (I/O)	ser port A TxClk / ser port A DCD / SPI port A enable	Timer2 I/O	LCD input clock	GPIO15	2
16	USB_ovr (I)	PFLT_ (O)		PORT16 (I/O)	USB overcurrent detect	1284 paper out/jam-duplicate		GPIO16	2
17 (HW strap)	USB_pwr (O)			PORT17 (I/O)	USB power relay control			GPIO17	2
18	CAM_rej (I)	CLPOWER(O)	EIRQ3 (I)	PORT18 (I/O)	10/100 CAM Reject	LCD power enable	Ext IRQ3-duplicat	GPIO18	4
19 (HW strap)	CAM_req (O)	CLLP (O)	DACK1 (O)	PORT19 (I/O)	10/100 CAM Req	LCD line/horz sync	DMA ch 1 Ack-duplicat	GPIO19	4
20	DTRC_ (O)	CLCP (O)		PORT20 (I/O)	ser port C DTR	LCD clock		GPIO20	8
21	DSRC_ (I)	CLFP (O)		PORT21 (I/O)	ser port C DSR	LCD fram pulse/ vert sync		GPIO21	4
22	RxCC (I/O) / RIC_ (I) / SPIC_CK(I/O)	CLAC (O)		PORT22 (I/O)	ser port C RxClk / ser port C RI / SPI port C Clk	LCD AC bias/data enable		GPIO22	4
23	TxCC (I/O) / DCDC_ (I) / SPIC_EN(I/O)	CLLE (O)		PORT23 (I/O)	ser port C TxClk / ser port C DCD / SPI port C enable	LCD line end signal		GPIO23	4
24	DTRD_ (O)	CLD[0](O)		PORT24 (I/O)	ser port D DTR	LCD data bit 0		GPIO24	4
25	DSRD_ (I)	CLD[1](O)		PORT25 (I/O)	ser port D DSR	LCD data bit 1		GPIO25	4
26	RxCD (I/O) /	CLD[2](O)	TIMER3 (I/O)	PORT26	ser port D RxClk /	LCD data bit 2	Timer3 I/O	GPIO26	4
27	TxCD (I/O) /	CLD[3](O)	TIMER4 (I/O)	PORT27	ser port D TxClk /	LCD data bit 3	Timer4 I/O	GPIO27	4
28	EIRQ1 (I)	CLD[4](O)	CLD[8] (O)	PORT28	Ext IRQ1-duplicat	LCD data bit 4	LCD data bit 8-	GPIO28	4
29	TIMER5 (I/O)	CLD[5](O)	CLD[9] (O)	PORT29	Timer5 I/O	LCD data bit 5	LCD data bit 9-	GPIO29	4

30	TIMER6 (I/O)	CLD[6](O)	CLD[10](O)	PORT30 (I/O)	Timer6 I/O	LCD data bit 6	LCD data bit 10-dupl	GPIO30	4
31	TIMER7 (I/O)	CLD[7](O)	CLD[11](O)	PORT31 (I/O)	Timer7 I/O	LCD data bit 7	LCD data bit 11-dupl	GPIO31	4
32	EIRQ2 (I)	PD0 (I/O)	CLD[8](O)	PORT32	Ext IRQ 2	1284 Data 0	LCD data bit 8	GPIO32	4
33		PD1 (I/O)	CLD[9](O)	PORT33		1284 Data 1	LCD data bit 9	GPIO33	4
34	iic_scl (I/O)	PD2 (I/O)	CLD[10](O)	PORT34	I2C clock	1284 Data 2	LCD data bit 10	GPIO34	4
35	iic_sda (I/O)	PD3 (I/O)	CLD[11](O)	PORT35	I2C data	1284 Data 3	LCD data bit 11	GPIO35	4
36	PWM_0 (O)	PD4 (I/O)	CLD[12](O)	PORT36	Pulse Width Modulator	1284 Data 4	LCD data bit 12	GPIO36	4
37	PWM_1 (O)	PD5 (I/O)	CLD[13](O)	PORT37	Pulse Width Modulator	1284 Data 5	LCD data bit 13	GPIO37	4
38	PWM_2 (O)	PD6 (I/O)	CLD[14](O)	PORT38	Pulse Width Modulator	1284 Data 6	LCD data bit 14	GPIO38	4
39	PWM_3 (O)	PD7 (I/O)	CLD[15](O)	PORT39	Pulse Width Modulator	1284 Data 7	LCD data bit 15	GPIO39	4
40	TxDC (O)	EIRQ3 (I)	CLD[16](O)	PORT40	ser port C TxData /	Ext IRQ 3	LCD data bit 16	GPIO40	4
41	RxDC (I)		CLD[17](O)	PORT41 (I/O)	ser port C RxData / SPI port C din		LCD data bit 17	GPIO41	4
42	RTSC_ (O)		USB_VP (I/O)	PORT42 (I/O)	ser port C RTS		USB Data +	GPIO42	4
43	CTSC_ (I)	PDIR (O)	USB_VM (I/O)	PORT43 (I/O)	ser port C CTS	1284 xceiver direction control	USB Data -	GPIO43	4
44 (HW strap)	TxDD (O)	PSELO_(O)	USB_OE_n (O)	PORT44 (I/O)	ser port D TxData / SPI port D dout	1284 periph on line	USB Tx Output Enable	GPIO44	4
45	RxDD (I)	PSTB_ (I/O)	USB_RCV (I)	PORT45 (I/O)	ser port D RxData / SPI port D din	1284 data strobe	USB Rx Data	GPIO45	4
46	RTSD_ (O)	PAFD_ (I)	USB_RXP (I)	PORT46 (I/O)	ser port D RTS	1284 auto line feed	(Fairchild phy only)	GPIO46	4
47	CTSD_ (I)	PINT_ (I)	USB_RXM (I)	PORT47 (I/O)	ser port D CTS	1284 initialize	(Fairchild phy only)	GPIO47	4
48	USB_SPND (O)	PSELI_(I)	DREQ1 (I)	PORT48 (I/O)	USB Suspend	1284 periph select	DMA channel 1 Req	GPIO48	2
49 (HW strap)	USB_SPEED (O)	PLH (O)	DONE1 (O)	PORT49 (I/O)	USB Speed	1284 periph logic high	DMA channel 1 Done	GPIO49	2
50	mdio(I/O)	USB_VP (I/O)		PORT50	MII/RMII management		duplicate	GPIO50	2
51	rx_dv(I)	USB_VM (I/O)		PORT51	MII rx data valid		USB Data -	GPIO51	2
52	rx_er(I)	USB_OE_n (O)		PORT52	MII rx error		USB Tx Output Enable duplicate	GPIO52	2
53	rxd[0](I)	USB_RCV (I)		PORT53	MII/RMII rx data bit		duplicate	GPIO53	2
54	rxd[1](I)	USB_SPND (O)		PORT54	MII/RMII rx data bit		duplicate	GPIO54	2
55	rxd[2](I)	USB_SPEED (O)		PORT55	MII rx data bit 2		USB Speed	GPIO55	2
56	rxd[3](I)	USB_RXP (I)		PORT56	MII rx data bit 3		(Fairchild phy only) duplicate	GPIO56	2
57	tx_en(O)	USB_RXM (I)		PORT57	MII/RMII tx enable		(Fairchild phy only) duplicate	GPIO57	2
58	tx_er(O)			PORT58	MII tx error			GPIO58	2
59	txd[0](O)			PORT59	MII/RMII tx data bit			GPIO59	2
60	txd[1](O)			PORT60	MII/RMII tx data bit			GPIO60	2
61	txd[2](O)			PORT61	MII tx data bit 2			GPIO61	2
62	txd[3](O)			PORT62	MII tx data bit 3			GPIO62	2
63	col(I)			PORT63	MII collision			GPIO63	2
64	crs(I)			PORT64	MII/RMII carrier			GPIO64	2
65	enet_phy_int_in(I)			PORT65	MII/RMII enet phy			GPIO65	2
66	mpmcaddrout[22](O)			PORT66	mem address bit 22			GPIO66	8
67	mpmcaddrout[23](O)			PORT67	mem address bit 23			GPIO67	8
68	mpmcaddrout[24](O)	mpmcckeout[0]	EIRQ0 (I)	PORT68	mem address bit 24	SDRAM clock enable	Ext IRQ0-duplicat	GPIO68	8
69	mpmcaddrout[25](O)	mpmcckeout[1]	EIRQ1 (I)	PORT69	mem address bit 25	SDRAM clock enable	Ext IRQ1-duplicat	GPIO69	8
70	mpmcaddrout[26](O)	mpmcckeout[2]	iic_scl (I/O)	PORT70	mem address bit 26	SDRAM clock enable	I2C clock -	GPIO70	8

71	mpmcaddrout[27](I	mpmcckeout[3]	iic_sda (I/O)	PORT71	mem address bit 27	SDRAM clock enable	I2C data -duplicat	GPIO71	8
72	ns_ta_strb(I)			PORT72	mem slow periph ack			GPIO72	8