Module DIMM-520_2

Hardware Reference Manual

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Release of Document: March 12, 2002
Filename: ModuleDIMMc.doc
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1. Introduction

The module DIMM-520 with its integrated and optional peripherals, based on the 32 Bit AMD ÉlanSC520 microcontroller, is designed for medium to high performance applications in telecommunication, data communication and information appliances on the general embedded market. This module has been designed on the SO-DIMM standard. It can easily be plugged on customized boards.

The AMD ÉlanSC520 microcontroller combines a low voltage 586 CPU running on 133 MHz, including FPU (Floating Point Unit) with a set of integrated peripherals: 32 Bit PCI controller, SDRAM controller for up to 256 MByte, GP (General Purpose) bus with programmable timing and ROM/Flash controller. Enhanced PC compatible peripherals like DMA controller, two UARTs and battery buffered RTC and CMOS, watchdog and software timers make this device a very fast system for both real time and PC/AT compatible applications.

Insyde Software's Mobile BIOS is available which offers serial and parallel remote features (video, keyboard, floppy). Furthermore FS FORTH-SYSTEME has adapted Datalight Sockets (TCP/IP Stack), ROM-DOS and the Flash File System FlashFX to this environment.

The DIMM-520 offers the software engineer the possibility to reduce the time-to-market phase even more. FS FORTH-SYSTEME added several features on-board as SDRAM (up to 64 MByte), PCI Fast Ethernet controller to facilitate networking and remote control. The enhanced JTAG port for low-cost debugging is supported. This allows instruction tracing during execution. A Strata-FLASH for booting and data is included on board. Hard disk is supported and a Super-I/O offers one parallel, two serial ports and controls floppy and keyboard. The internal serial ports are not connected.

FS FORTH-SYSTEME has adapted Windows CE 3.0 to this platform and offers drivers and support. With Ethernet debugging the software designer has powerful means for fast debugging his applications.

Due to the 16 MByte FLASH it is possible to realize larger, complete systems on this module like Linux, QNX or VxWorks.

2. Features

DIMM-520 is designed to be a member of the DIMM-PC® family. The features of the DIMM-520 are:

- **16 MByte STRATA-FLASH or 2 MByte AMD FLASH**
- **64 MByte or 16 MByte SDRAM**
- **Super-I/O FDC37B727 with 2 serial COM-Ports 1 parallel port and keyboard signals. Mouse signals are not connected.**
- **PCI Ethernet controller with EEPROM. Rx and Tx signals are provided on an additional connector X3.**
- **Enhanced JTAG port. On-board connector X1.**
- **BIOS for ÉlanSC520 by Insyde Software Inc. Including serial or parallel remote features (Video, Keyboard, Floppy).**

3. Functional Description

3.1. CPU AMD ÉlanSC520

The CPU AMD ÉlanSC520 is powered with 2.5V (core and analog path) and 3.3V (all other voltages) except VRTC, which is powered with about 3V either from battery or from on-board 3.3V. This voltage is limited to 3.3V, the other 3.3V power planes have a limit of 3.6V.

The CPU is clocked with a 32.768 KHz quartz. An internal PLL derives from this frequency the RTC clock and DRAM refresh clock and the clocks for PC/AT compatible PIT (1.1882 MHz) and UARTs (18.432 MHz). All other stages (CPU, PCI, GP bus, GP DMA, ROM, SSI, timers) are fed from the second clock generator driven by a 33.33 MHz clock oscillator. SDRAM is clocked with 66.66 MHz.

3.2. SDRAM stage

The SDRAM (up to 64 MByte on-board) has its own DRAM bus containing memory addresses MA0..12, memory data MD0..31 and control signals for up to four banks. Due to small load no buffering of clocks and signals is necessary.

3.3. ROM stage

ROM or FLASH are driven by the general purpose address bus GPA0..25. It has three programmable chip selects with each up to 64 MByte range. The ROM Data bus is either the 32 bit general purpose bus GPD0..31 or the memory data bus MD0..31. Configuration pins decide, which bus at boot time is used. The bus size is selectable with 8, 16 or 32 bit. The DIMM-520 has a FLASH IC for up to 16 MByte 16 bit ROM or FLASH selected by BOOTCS# connected to MD0..16.

3.4. 32 I/O Ports

The ÉlanSC520 CPU has 32 I/O ports. They have alternate functions. Most of them are control signals for GP bus (PIO0..26) used as ISA-bus. PIO27 (GPCS0#) is used as a programmable external chip select and PIO28,29 are not connected. PIO30,31 are used to drive a serial parameter EEPROM on-board.

3.5. 2 kByte EEPROM for BIOS and Applications on PIO30,31

An on-board serial EEPROM with 2 kByte and I²C bus is controlled by PIO30 (I2CDAT) and PIO31 (I2CCLK). 128 byte are used for non-volatile BIOS defaults, the remaining range may contain application specific data and parameters. The BIOS contains calls to read and write to this memory (see BIOS documentation).

3.6. On-board Power Supply fed by +5V

All voltages on-board are generated from +5V.

The switching regulator U9 generates +3.3V and +2.5V from +5V for all stages on the DIMM-520.

A battery buffers RTC in the CPU AMD ÉlanSC520. An external battery may be connected. Battery status is controlled by BBATSEN, which sets a power fail bit in a status register for RTC, if BBATSEN is low at power-up.

3.7. Voltage Supervision, RESET Generation

Three voltages are used on board: +2.5V, +3.3V and +5V. U9 controls +2.5 and +3.3V. 1RESET# or 2RESET# will become active low, if these voltages are out of tolerance. An external PGOOD is wired or-ed to U10. It can also be activated from extended JTAG signal SRESET# via X1. The wired OR of 1RESET# and 2RESET# control U10. Its output PWRGOOD is low (not active), if either the signals described above from U10 are low or +5V is out of tolerance. Typical length of PWRGOOD low is greater than 1 sec (minimum 790 msec).

3.8. Serial Ports

The AMD ÉlanSC520 CPU has two internal asynchronous ports and one synchronous serial port. None of these ports are used.

3.9. Fast Ethernet Controller Stage

Connected to the PCI bus device 0 (REQ/GNT0#) of the Élan SC520 CPU, a Fast Ethernet Controller U7 supports 10/100Mbps transfer depending on driver software. X3 is a JST B5B-PH-SM3 5 pin connector. Parameters as physical address and magic packet mode are stored in a 64X16 bit Serial EEPROM controlled by U7. 2 status LEDs LE1, LE2 show the state of the Ethernet connection. For a more detailed hardware and software description see Intel 82559ER manual.

3.10. GP Bus used for ISA Bus

The AMD ÉlanSC520 CPU contains an 8/16bit General Purpose Bus (GP bus) with 26 address lines (GPA0..25), 16 data lines (GPD0..15) and different control lines using PIO ports in their alternate GP bus function. Its timing is programmable for speeds up to 33MHz. This bus is to emulate a 16 bit ISA bus (PC/104) running with 8 MHz. ISA bus signal are connected without buffers directly to the lines of the CPU due to the 5V tolerance of the 3.3V signals.

8 bit signals SMEMRD# and SMEMWR# (active only at addresses beyond 1 MByte) are not supported (GPMEM_RD# and GPMEM_WR# used).

The AMD ÉlanSC520 CPU has only 4 DMA channels on GP bus. DMA channel 2 is used for Super-I/O (U2). All four channels are connected to edge connector X2.

Not supported ISA bus signals: 0WS#, IOCHK#, IRQ15, REFRESH#, 8MHz and 14.318 MHz clocks, MASTER#.

SMISW# is not supported on DIM-520.

3.11. IDE Hard Disk support

IDE signals are derived from GP bus signals without buffers for the data signals IDED0..15. IDECS0,1 are hard wired to GPCS6,7.

3.12. Super-I/O with Floppy, Ports, Keyboard, Mouse

Connected to the GP bus running as ISA bus the Super I/O U2 provides two serial ports, a parallel port, floppy and PS/2 keyboard.

The two serial ports support baud rates up to 460 800 baud. They support both all 8 PC/AT compatible signals. All signal are connected to X2.

The parallel port signals are connected to X2.

A detailed description of the Super I/O hardware and registers see FDC37B727 datasheet (37b72x.pdf).

3.13. Enhanced JTAG

The DIMM-520 has one JTAG connector on-board. X1 is a 20-pin JTAG connector wired with U1 (CPU). The standard JTAG supports TMS, TCK, TRST#, TDI and TDO.

X1 supports ÉlanSC520 CPU with enhanced JTAG functionality. Besides the above mentioned signals this JTAG supports SRESET#, CMDACK, BR/TC, TRIG/TRACE and STOP/TX signals.

For a detailed description see AMD ÉlanSC520 manuals.

4. Connectors Of DIMM-520

4.1. Edge Connector X2

Pin	Function	I/O	PU/PD	Pin	Function	I/O	PU/PD
1	reserved IOCHK#	I	nc	2	GND	P	
3	GPRESET	O		4	IDECS0#	O	
5	GPD7	I/O		6	VCC (+5V)	P	
7	GPD6	I/O		8	IDECS1#	O	
9	IRQ9	I		10	not connected		
11	GPD5	I/O		12	not connected		
13	GPD4	I/O		14	DTR2#	O	-
15	DRQ2	I		16	RIN2#	I	-
17	GPD3	I/O		18	TXD2	O	-
19	GPD2	I/O		20	CTS2#	I	-
21	GPMEM_CS16#	I	PU 1k	22	RXD2	I	-
23	GPD1	I/O		24	RTS2#	O	-
25	reserved 0WS#	I	PU 1k	26	DCD2#	I	-
27	GPIO_CS16#	I	PU 1k	28	GND	P	
29	GPD0	I/O		30	DSR2#	I	
31	GPBHE#	O		32	FDHDSEL#	O	
33	GPRDY	I	PU3 4k7	34	FDRDATA#	I	PU 1k5
35	IRQ10	I		36	FDWRPRT#	I	PU 1k5
37	GPAEN	O		38	FDTRK0#	I	PU 1k5
39	GPMEM_WR#	O		40	FDWGATE#	O	
41	IRQ11	I	PU3 10k	42	FDWDATA#	O	
43	GPA19	O		44	FDSTEP#	O	
45	GPMEM_RD#	O		46	FDDIR#	O	
47	IRQ12	I		48	FDMTR0#	O	PU 1k5
49	GPA18	O		50	FDDSKCHG#	I	PU 1k5
51	GPIOWR#	O		52	FDDS0#	O	PU 1k5
53	reserved IRQ15	I	nc	54	FDCIDX#	I	PU 1k5
55	GPA17	O		56	not connected		
57	GPIORD#	O		58	GND	P	-
59	IRQ14	I		60	GPA16	O	
61	DACK0#	O		62	GND	P	
63	GPA15	O		64	not connected		

Pin	Function	I/O	PU/PD	Pin	Function	I/O	PU/PD
65	DRQ0	I		66	VCC (+5V)	P	-
67	GPA14	O		68	ACTLED#		
69	DACK5#	O		70	LILED#		
71	GPA13	O		72	I2CDAT	I/O	PU 4k7
73	DRQ5	I		74	I2CCLK	O	PU 4k7
75	GPA12	O		76	GPCS0#	O	
77	reserved REFRESH#	O	PU 10k	78	DCD1#	I	
79	GPD8	I/O		80	DSR1#	I	
81	GPA11	O		82	RXD1	I	
83	reserved 8MHz (nc)	O	-	84	RTS1#	O	PD 1k
85	GPD9	I/O		86	TXD1	O	
87	GPA10	O		88	CTS1#	I	
89	IRQ7	I		90	GND	P	
91	GPD10	I/O		92	DTR1#	O	
93	GPA9	O		94	RIN1#	I	
95	IRQ6	I		96	STB#	O	
97	GPD11	I/O		98	AFD#	O	
99	GPA8	O		100	PD0	I/O	
101	IRQ5	I		102	ERR#	I	
103	GPD12	I/O		104	PD1	I/O	
105	GPA7	O		106	INIT#	O	
107	IRQ4	I		108	PD2	I/O	
109	DACK7#	O		110	SLIN#	I	
111	DRQ7	I		112	PD3	I/O	
113	IRQ3	I		114	PD4	I/O	
115	GPA6	O		116	PD5	I/O	
117	GPD13	I/O		118	PD6	I/O	
119	DACK2#	O		120	PD7	I/O	
121	GPA5	O		122	ACK#	O	
123	GPD14	I/O		124	BUSY#	I	
125	GPTC	O		126	PE	I	
127	GPA4	O		128	SLCT#	I	

Pin	Function	I/O	PU/PD	Pin	Function	I/O	PU/PD
129	GPD15	I/O		130	KBDAT	OC	PU3 10k
131	GPALE	O		132	KBCLK	OC	PU3 10k
133	GPA3	O		134	SPEAKER	O	
135	reserved MASTER#	I	PU 10k	136	PGOOD	I	
137	GPA2	O		138	not connected		
139	GPA1	O		140	VCC (+5V)	P	
141	OSC14.318	O		142	VBAT	P	
143	GPA0	O		144	GND	P	

OC = Open Collector

PD = Pull Down

PD CPU = Pull Down internal to CPU, see ÉlanSC520 data sheet

PU = Pull Up (to 5V)

PU3 = Pull Up to 3.3V

PU CPU = Pull Up internal to CPU, see ÉlanSC520 data sheet

P = Power Pin

4.2. JTAG-Connector X1

Pin	Function	I/O	Pin	Function	I/O
1	GND	Power	2	VCC (+3.3V)	Power
3	TCK	I	4	GND	Power
5	TMS	I	6	GND	Power
7	TDI	I	8	GND	Power
9	TDO	O	10	GND	Power
11	TRST#	I	12	GND	Power
13	SRESET#	I	14	GND	Power
15	CMDACK	O	16	GND	Power
17	BR/TC	I	18	TRIG/TRACE	O
19	STOP/TX	O	20	not connected (key)	

4.3. Ethernet-Connector X3

Pin	Function	I/O
1	TD+	O
2	TD-	O
3	RD+	I
4	RD-	I
5	GND	Power

5. Members of the DIMM-520 family

Product	Flash	SDRAM
325	8M*16, Strata (=16 MByte)	2*4M*16 (=16 MByte)
326	1M*16, AMD (=2 MByte)	2*4M*16 (=16 MByte)
327	8M*16, Strata (=16 MByte)	2*16M*16 (=64 MByte)