ModNET50 Module

Hardware Reference Manual

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1. General

This Manual describes the ModNET50 module, one of a family of modules based on NetSilicon's NET+ARM family of microcontrollers. The module approach has several advantages over a full custom design.

- Complete family support for NET+40, NET+50 and further derivatives.
- The module interface does not change, if any package of any part of the module changes. Future CPUs may have a BGA package. Compatible derivatives may have a different package. Memory parts may have different packages.
- Long term stability and availability.
- Newer derivatives will be less expensive, since they use newer technology (NET+50 is less expensive than the NET+40)
- Adaptation to application's performance requirements (speed, memory size) by simply changing the module variant.
- Higher complexity module will need advanced board technology (fine pitch/layers). Size of module will optimize the overhead.

2. Features

- Module with NetSilicon's NET+50 in PQFP208 package clocked at 44MHz
- Voltage requirement 3.3V (additional 5V needed if CAN controller is assembled)
- 32-bit SDRAM, one bank of 16 MBytes
- 16-bit Flash
- PHY on module (transformer and RJ45 on base board)
- 2 serial interfaces, LVTTL level (line driver on base board)
- Serial 8-KByte EEPROM for storing configuration parameters
- RTC
- Reset controller
- 512 KBytes of SRAM with battery backup

3. Module Definition

3.1. Power Supply

The main power supply for the module is 3.3V. Lower core voltages, such as required for the NET+50, are generated on the module.

The CAN controller needs 5V, because there is no standalone CAN controller available which works with 3.3V. For this part, 5V must be connected to the module.

The pins of the NET+40 and NET+50 are not 5V tolerant. Some signals (16-bit data, 20-bit address bus and control bus) are buffered before they leave the module. See section 4.2 “System Connector X2” for a list of those signals which are 5V tolerant.

3.2. Reset Controller

The modules main power supply (3.3V) is monitored by the reset controller. An external reset source, i.e. push button, can be connected to the module. The 5V power supply should be monitored on the base board.

3.3. CPU

The module is designed to be assembled with a NET+50 or NET+40-4 microcontroller.

3.4. System Clock

Starting with revision 4 of the NET+40 (P/N 0136974) the on-chip PLL is fully functional. The system clock (SYSCLK) is generated from an external oscillator running at 18.432 MHz.

The PLL's multiplication factor is controlled via software. The following frequencies can be generated:

PLLCNT	F_{SYSCLK}	Remarks
3	22.1184 MHz	
4	25.8048 MHz	
5	29.4912 MHz	
6	33.1776 MHz	used for the NET+40
7	36.8640 MHz	
8	40.5504 MHz	
9	44.2368 MHz	used for the NET+50
10	47.9232 MHz	
11	51.6096 MHz	
12	55.2960 MHz	
13	58.9824 MHz	
14	62.6688 MHz	
15	66.3552 MHz	

If a NET+50 is assembled, the speed can be changed easily by writing a different value to the PLL configuration register.

3.5. Flash Memory

There is one 16-bit boot flash on the module. Maximum Flash size is 8 Mbytes. The following chips can be assembled: 29LV800, 29LV160, 29DL32x, 29LV641.

3.6. SDRAM

There is one SDRAM bank on the module. Memory size is limited to 16 Mbytes. The NET+50 only supports chips with 8 CAS lines.

3.7. Ethernet

The Ethernet MAC is already included in the NET+ARM CPU. The PHY for the 100BaseT is on the module.

The transformer is not on the module. In most application this transformer must be located near to the RJ45 connector.

Two LEDs may be connected to module pins: One (LEDLNK) to show link and activity and a second (LEDH) to indicate 100 Mbit/sec operation.

There are pins reserved for a second Ethernet interface.

3.8. EEPROM

The system needs to be able to store configuration data, e. g. the Ethernet's MAC address. On the module there is an 8-KByte EEPROM with an I²C interface for this purpose.

The I²C bus is implemented on the NET+ARM by emulating open drain outputs in software. The GPIO pins are switched to input to get a passive high level. The high level of this bus is 3.3V.

The current size of the EEPROM is 8KBytes. Most of this nonvolatile memory is available for the user's application, but some bytes are already defined.

Address	Function	Description
100h	ucCheckSum	Checksum, sum of all bytes from 100h to 13Fh must be zero.
101h	ucFlags	various flag. Bit 0: no gateway = 0 (aucGateWay invalid), use gateway = 1 (aucGateWay valid)
102h	ucRegistry	Not used with ModNET
103h	ucUseDHCP	0 -> DHCP off 01h..0FFh -> DHCP on
104h 109h	aucMacAddress[6]	MAC Address, MSB first, the bytes 104h, 105h and 106h must contain the values 00h, 04h, 0F3h (=FS Forth-Systeme).
10Ah 10Dh	aucIpAddress[4]	IP Address, MSB 1st
10Eh 111h	aucSubnetMask[4]	Subnet Mask, MSB 1st
112h 115h	aucGateWay[4]	Gateway IP address, MSB 1st
116h 119h	aucDNS[4]	Address of Domain Name Server
11Ah 11Dh	aucBroadcastAddr[4]	Broadcast Address
11Eh 121h	aucIpAddrPpp1[4]	PPP COM1 IP Address
122h 125h	aucIpAddrPpp2[4]	PPP COM2 IP Address
126h 129h	aucIpAddrPpp1peer [4]	PPP COM1 Peer IP Address
12Ah 12Dh	aucIpAddrPpp2peer [4]	PPP COM2 Peer IP Address
12Eh 13Fh	aucReserved[18]	Reserved, not used

3.9. Peripheral Bus

In order to connect additional peripherals to the NET+ARM, a peripheral bus is available on the module's connector. This bus is 5V tolerant.

The signals BE3# and BE2# are available on module pins to allow 8-bit (read) accesses to 16-bit peripherals.

There are two free chip selects (CS3# and CS4#) to select peripherals.

3.10. CAN Controller

On the module there is an Infineon TwinCAN 82C900 (Dual CAN Controller).

This controller needs a multiplexed 8-bit address/data bus. Since the NET+50 (and NET+40) does not support a multiplexed bus, two 8-bit buffers and some glue logic is used to generate the multiplexed signals. Buffers additionally isolate the 3V NET+50 signals from the 5V CAN controller signals.

3.11. RTC

To save board space an RTC with I²C interface is used. The RTC is powered either with battery power or the 3.3V power supply. The battery for the RTC is on the main board. Battery power switch over is on the module.

The I²C bus is implemented on the NET+ARM by emulating open drain outputs in software. The GPIO pins are switched to input to get a passive high level. The high level of this bus is 3.3V.

The RTC used is: Philips PCF8563, I²C, 400 kHz, 3.3V or 5V, Interrupt-Output, SO8, -40..+85°

3.12. SRAM

A 512k*8 SRAM is on the module. This SRAM is with battery backup, and is able to hold nonvolatile application information.

4. Module Pins

4.1. System Connector X2

Pin	Signal	2nd func.	3rd func.	Type	5V tol.	Description
X2-39	RSTIN#	-	-	I	no	Reset input
X2-41	PWRGOOD	-	-	O	no	Output of the reset controller
X2-67	BCLK	-	-	O	yes	System Clock
X2-66	TS#	-	-	O	no	Transfer Start, not available on module ModNET_0
X2-68	TA#	-	-	O	no	Data Transfer Acknowledge
X2-70	TEA#	TLAST#	-	O	no	Data Transfer Error Acknowledge
X2-75	BE3#	-	-	O	yes	
X2-73	BE2#	-	-	O	yes	
X2-65	R/W#	-	-	O	yes	
X2-61	WE#	-	-	O	yes	
X2-63	OE#	-	-	O	yes	
X2-79	CS2#	-	-	O	yes	Used on the module to select SRAM and CAN, see signal CSMODE
X2-69	CS3#	-	-	O	yes	External chip select, see signal CSMODE
X2-71	CS4#	-	-	O	yes	External chip select, see signal CSMODE
-	CS5#	-	-	O	-	Reserved
-	CS6#	-	-	O	-	Reserved
-	CS7#	-	-	O	-	Reserved
X2-71	BR#	-	-	I/O	no	Bus Request
X2-72	BG#	-	-	I/O	no	Bus Grant
X2-76	BUSY#	-	-	I/O	no	Bus Busy
X2-81	D16	-	-	I/O	yes	Data Bus
X2-83	D17	-	-	I/O	yes	Data Bus
X2-85	D18	-	-	I/O	yes	Data Bus
X2-87	D19	-	-	I/O	yes	Data Bus
X2-89	D20	-	-	I/O	yes	Data Bus
X2-91	D21	-	-	I/O	yes	Data Bus
X2-93	D22	-	-	I/O	yes	Data Bus
X2-95	D23	-	-	I/O	yes	Data Bus
X2-97	D24	-	-	I/O	yes	Data Bus

Pin	Signal	2nd func.	3rd func.	Type	5V tol.	Description
X2-99	D25	-	-	I/O	yes	Data Bus
X2-101	D26	-	-	I/O	yes	Data Bus
X2-103	D27	-	-	I/O	yes	Data Bus
X2-105	D28	-	-	I/O	yes	Data Bus
X2-107	D29	-	-	I/O	yes	Data Bus
X2-109	D30	-	-	I/O	yes	Data Bus
X2-111	D31	-	-	I/O	yes	Data Bus
X2-7	A0	-	-	O	yes	Address Bus
X2-9	A1	-	-	O	yes	Address Bus
X2-11	A2	-	-	O	yes	Address Bus
X2-13	A3	-	-	O	yes	Address Bus
X2-15	A4	-	-	O	yes	Address Bus
X2-17	A5	-	-	O	yes	Address Bus
X2-19	A6	-	-	O	yes	Address Bus
X2-21	A7	-	-	O	yes	Address Bus
X2-23	A8	-	-	O	yes	Address Bus
X2-25	A9	-	-	O	yes	Address Bus
X2-27	A10	-	-	O	yes	Address Bus
X2-29	A11	-	-	O	yes	Address Bus
X2-31	A12	-	-	O	yes	Address Bus
X2-33	A13	-	-	O	yes	Address Bus
X2-35	A14	-	-	O	yes	Address Bus
X2-37	A15	-	-	O	yes	Address Bus
X2-45	A16	-	-	O	yes	Address Bus
X2-47	A17	-	-	O	yes	Address Bus
X2-49	A18	-	-	O	yes	Address Bus
X2-51	A19	-	-	O	yes	Address Bus
X2-36	CFG4	-	-	I	no	Connected to A13, = System Status Register Bit 4
X2-38	CFG5	-	-	I	no	Connected to A14, = System Status Register Bit 5
X2-40	CFG6	-	-	I	no	Connected to A15, = System Status Register Bit 6
X2-42	CFG7	-	-	I	no	Connected to A16, = System Status Register Bit 7
X2-80	CFG8	-	-	I	no	Connected to A17, = System Status Register Bit 8
X2-82	CFG9	-	-	I	no	Connected to A18, = System Status Register Bit 9
X2-84	CFG10	-	-	I	no	Connected to A19, = System Status

Pin	Signal	2nd func.	3rd func.	Type	5V tol.	Description
						Register Bit 10
X2-5	LITEND#	-	-	I	no	Low -> Little Endian Not available on module ModNET50_0
X2-6	CSMODE	-	-	I	yes	High -> CS3# and CS4# available for external use Low -> CS4# only available for external use Not available on ModNET50_0/ModNET50_1
X2-64	FLSH_DIS	-	-	I	no	Disable Flash on module. Needed to enter debugger, if Flash is empty. Not available on module ModNET50_0
X2-56	TCK	-	-	I	no	JTAG, not available on module ModNET50_0
X2-58	TMS	-	-	I	no	JTAG, not available on module ModNET50_0
X2-60	TDI	-	-	I	no	JTAG, not available on module ModNET50_0
X2-62	TDO	-	-	O	no	JTAG, not available on module ModNET50_0
X2-54	TRST#	-	-	I	no	JTAG, not available on Modnet50_0
X2-1	GND	-	-	P	-	
X2-2	GND	-	-	P	-	
X2-3	GND	-	-	P	-	
X2-4	GND	-	-	P	-	
X2-43	GND	-	-	P	-	
X2-44	GND	-	-	P	-	
X2-77	GND	-	-	P	-	
X2-113	GND	-	-	P	-	
X2-114	GND	-	-	P	-	
X2-115	GND	-	-	P	-	
X2-116	GND	-	-	P	-	
X2-117	+3.3V	-	-	P	-	
X2-118	+3.3V	-	-	P	-	
X2-119	+3.3V	-	-	P	-	
X2-120	+3.3V	-	-	P	-	

Peripheral Connector X3

Pin	Signal	2nd func.	3rd func.	Type	5V tol.	Description
X3-5	PORTA0	DCDA#	DONE1#	I/O	no	
X3-6	PORTA1	CTSA#		I/O	no	
X3-7	PORTA2	DSRA#	DACK1#	I/O	no	
X3-8	PORTA3	RXDA		I/O	no	
X3-9	PORTA4	RXCA#	OUT1A#	I/O	no	
X3-10	PORTA5	RTSA#		I/O	no	
X3-11	PORTA6	DTRA#	DREQ1#	I/O	no	
X3-12	PORTA7	TXDA		I/O	no	
X3-13	PORTB0	DCDB#	DONE2#	I/O	no	
X3-14	PORTB1	CTSB#	RPSF#	I/O	no	
X3-15	PORTB2	DSRB#	DACK2#	I/O	no	
X3-16	PORTB3	RXDB		I/O	no	
X3-17	PORTB4	RXCB	OUT1B#	I/O	no	
X3-18	PORTB5	RTSB#	REJECT#	I/O	no	
X3-19	PORTB6	DTRB#	DREQ2#	I/O	no	
X3-20	PORTB7	TXDB		I/O	no	
X3-21	PORTC0	CI0		I/O	no	ModNET50_1/ModNET50_1: Used as Interrupt Input from PHY ModNET50_2: Used for SDRAM reset bugfix
X3-22	PORTC1	CI1		I/O	no	Used as Interrupt Input from RTC
X3-23	PORTC2	CI2		I/O	no	Used as Interrupt Input from CAN
X3-24	PORTC3	CI3	AMUX	I/O	no	
X3-25	PORTC4	RIB#	RESET#	I/O	no	ModNET50_0: Reset Output to PHY and CAN Controller ModNET50_1: Reset for CAN Controller
X3-26	PORTC5	TXCB	OUT2B#	I/O	no	ModNET50_0: I2CCLK, Used as I²C clock ModNET50_1: free
X3-27	PORTC6	RIA#	IRQ#	I/O	no	ModNET50_0: Used for SDRAM reset bug fix ModNET50_1: I2CCLK, Used as I²C clock
X3-28	PORTC7	TXCA	OUT2A#	I/O	no	I2CDAT, Used as I²C data
X3-29	PORTD0			I/O	-	Reserved

X3-30	PORTD1			I/O	-	Reserved
X3-31	PORTD2			I/O	-	Reserved
X3-32	PORTD3			I/O	-	Reserved
X3-33	PORTD4			I/O	-	Reserved
X3-34	PORTD5			I/O	-	Reserved
X3-35	PORTD6			I/O	-	Reserved
X3-36	PORTD7			I/O	-	Reserved
X3-37	PORTE0			I/O	-	Reserved
X3-38	PORTE1			I/O	-	Reserved
X3-39	PORTE2			I/O	-	Reserved
X3-40	PORTE3			I/O	-	Reserved
X3-41	PORTE4			I/O	-	Reserved
X3-42	PORTE5			I/O	-	Reserved
X3-43	PORTE6			I/O	-	Reserved
X3-44	PORTE7			I/O	-	Reserved
X3-65	PACK#	PCLKD1	GPIOF7	I/O	no	
X3-67	PEN#	PCLKD2	GPIOF6	I/O	no	
X3-69	PINT1#	PCLKD3	GPIOF5	I/O	no	
X3-71	PINT2#	PCLKD4	GPIOF4	I/O	no	
X3-75	PDATA0	-	GPIOD0	I/O	no	
X3-77	PDATA1	-	GPIOD1	I/O	no	
X3-79	PDATA2	-	GPIOD2	I/O	no	
X3-81	PDATA3	-	GPIOD3	I/O	no	
X3-83	PDATA4	-	GPIOD4	I/O	no	
X3-85	PDATA5	-	GPIOD5	I/O	no	
X3-87	PDATA6	-	GPIOD6	I/O	no	
X3-89	PDATA7	-	GPIOD7	I/O	no	
X3-91	PDATA8	POE1#	-		no	
X3-93	PDATA9	POE2#	-		no	
X3-95	PDATA10	POE3#	-		no	
X3-97	PDATA11	POE4#	-		no	
X3-99	PDATA12	PCLKC1#	-		no	
X3-101	PDATA13	PCLKC2#	-		no	
X3-103	PDATA14	PCLKC3#	-		no	
X3-105	PDATA15	PCLKC4#	-		no	
X3-107	PCS#	FAULT2#	GPIOG7	I/O	no	
X3-109	PRW#	FAULT3#	GPIOF0	I/O	no	
X3-111	PBRW#	FAULT4#	GPIOF1	I/O	no	
X3-76	PA0	ACK1#	GPIOH0	I/O	no	
X3-78	PA1	ACK2#	GPIOH1	I/O	no	
X3-80	PA2	ACK3#	GPIOH2	I/O	no	
X3-82	PA3	ACK4#	GPIOH3	I/O	no	

X3-84	PA4	BUSY1	GPIOH4	I/O	no	
X3-86	PA5	BUSY2	GPIOH5	I/O	no	
X3-88	PA6	BUSY3	GPIOH6	I/O	no	
X3-90	PA7	BUSY4	GPIOH7	I/O	no	
X3-92	PA8	PE1	GPIOG0	I/O	no	
X3-94	PA9	PE2	GPIOG1	I/O	no	
X3-96	PA10	PE3	GPIOG2	I/O	no	
X3-98	PA11	PE4	GPIOG3	I/O	no	
X3-100	PA12	PSELECT 1	GPIOG4	I/O	no	
X3-102	PA13	PSELECT 2	GPIOF3	I/O	no	
X3-104	PA14	PSELECT 3	GPIOF2	I/O	no	
X3-106	PA15	PSELECT 4	GPIOG5	I/O	no	
X3-108	PA16	FAULT1#	GPIOG6	I/O	no	
X3-48	TPIP1	-	-	I	-	Ethernet 1 Input+
X3-50	TPIN1	-	-	I	-	Ethernet 1 Input-
X3-52	TPOP1	-	-	O	-	Ethernet 1 Output+
X3-54	TPON1	-	-	O	-	Ethernet 1 Output-
X3-56	LEDLNK1	-	-	O	-	Ethernet 1 Line/Activity LED
X3-58	LEDH1	-	-	O	-	Ethernet 1 10/100 Mbit LED
X3-60	ESD1	-	-	I	-	Ethernet 1 Signal detect
X3-62	EVCC1	-	-	P	-	Ethernet 1 VCC, used for magnetics
X3-64	EGND1	-	-	P	-	Ethernet 1 GND
X3-47	TPIP2	-	-	I	-	Reserved for Ethernet 2 Input+
X3-49	TPIN2	-	-	I	-	Reserved for Ethernet 2 Input-
X3-51	TPOP2	-	-	O	-	Reserved for Ethernet 2 Output+
X3-53	TPON2	-	-	O	-	Reserved for Ethernet 2 Output-
X3-55	LEDLNK2	-	-	O	-	Reserved for Ethernet 2 Line/Activity LED
X3-57	LEDH2	-	-	O	-	Reserved for Ethernet 2 10/100 Mbit LED
X3-59	ESD2	-	-	I	-	Reserved for Ethernet 2 signal detect
X3-61	EVCC2	-	-	P	-	Reserved for Ethernet 2 VCC, used for magnetics
X3-63	EGND2	-	-	P	-	Reserved for Ethernet 2 GND
-	USBP	-	-	I/O	-	Reserved
-	USBN	-	-	I/O	-	Reserved

X3-66	CANH/TXDA	-	-	I/O	yes	CAN_TXD or CANH, channel A
X3-68	CANL/RXDA	-	-	I/O	yes	CAN_RXD or CANL, channel A
X3-70	CANH/TXDB	-	-	I/O	yes	CAN_TXD or CANH, channel B
X3-72	CANL/RXDB	-	-	I/O	yes	CAN_RXD or CANL, channel B
X3-1	GND	-	-	P	-	
X3-2	GND	-	-	P	-	
X3-45	GND	-	-	P	-	
X3-46	GND	-	-	P	-	
X3-73	GND	-	-	P	-	
X3-74	GND	-	-	P	-	
X3-113	GND	-	-	P	-	
X3-114	GND	-	-	P	-	
X3-115	GND	-	-	P	-	
X3-116	GND	-	-	P	-	
X3-117	+3.3V	-	-	P	-	
X3-119	+3.3V	-	-	P	-	
X3-3	+5V	-	-	P	-	
X3-4	+5V	-	-	P	-	
X3-117	VBAT	-	-	P	-	For backup of SRAM and RTC
X3-119	VBAT	-	-	P	-	For backup of SRAM and RTC