Mod520C_2

FORTH-SYSTEME GmbH

P.O. Box 11 03 ● D-79200 Breisach, Germany
Kueferstrasse 8 ● D-79206 Breisach, Germany
☎+49 (7667) 908-0 ● Fax +49 (7667) 908-200 ● e-mail: sales@fsforth.de

FS FORTH-SYSTEME GmbH
Postfach 1103, D-79200 Breisach a. Rh., Germany

Release of Document: May 27, 2004
Filename: Mod520C_2.doc
Author: Hans-Peter Schneider

Table of Contents

1. Introduction

The module MOD520C with its integrated and optional peripherals, based on the 32 Bit AMD ÉlanSC520 microcontroller, is designed for medium to high performance applications in telecommunication, data communication and information appliances on the general embedded market. It can easily be designed in customized boards.

The AMD ÉlanSC520 microcontroller combines a low voltage 586 CPU running on 133 MHz, including FPU (Floating Point Unit) with a set of integrated peripherals: 32 Bit PCI controller, SDRAM controller for up to 256 MByte, GP (General Purpose) bus with programmable timing and ROM/Flash controller. Enhanced PC compatible peripherals like DMA controller, two UARTs and battery buffered RTC and CMOS, watchdog and software timers make this device a very fast system for both real time and PC/AT compatible applications.

Insyde Software's Mobile BIOS is available which offers serial and parallel remote features (video, keyboard, floppy). Furthermore FS FORTH-SYSTEME has adapted Datalight Sockets (TCP/IP Stack), ROM-DOS and the Flash File System FlashFX to this environment.

The MOD520C offers the software engineer the possibility to reduce the time-to-market phase even more. FS FORTH-SYSTEME added several features on-board as SDRAM (up to 64 MByte), PCI Fast Ethernet controller to facilitate networking and remote control. A Strata-FLASH for booting and data is included on board. Two CAN Ports are additionally available for communication. 512 Kbyte SRAM is available for battery buffered data. The enhanced JTAG port for low-cost debugging is supported. This allows instruction tracing during execution.

FS FORTH-SYSTEME has adapted Windows CE 3.0 to this platform and offers drivers and support. With Ethernet debugging the software designer has powerful means for fast debugging his applications.

Due to the 16 MByte FLASH it is possible to build larger, complete systems on this module like Linux, QNX or VxWorks.

2. Features

- **16 MByte STRATA-FLASH or 2 MByte AMD FLASH**
- **64 MByte or 16 MByte SDRAM**
- **512 KByte battery buffered SRAM**
- **PCI Ethernet controller with EEPROM. Rx and Tx signals are provided on the System Connectors**
- **Two CAN-Buses.**
- **Enhanced JTAG port available on System Connector.**
- **GP-Bus signals available on System Connector**
- **PCI-Bus signals available on System Connector**
- **BIOS for ÉlanSC520 by Insyde Software Inc. Including serial or parallel remote features (Video, Keyboard, Floppy).**

3. Functional Description

3.1.1. CPU AMD ÉlanSC520

The CPU AMD ÉlanSC520 is powered with 2.5V (core and analog path) and 3.3V (all other voltages) except VRTC, which is powered with about 3V either from battery or from on-board 3.3V. This voltage is limited to 3.3V, the other 3.3V power planes have a limit of 3.6V.

The CPU is clocked with a 32.768 kHz quartz. An internal PLL derives from this frequency the RTC clock and DRAM refresh clock and the clocks for PC/AT compatible PIT (1.1882 MHz) and UARTs (18.432 MHz). All other stages (CPU, PCI, GP bus, GP DMA, ROM, SSI, timers) are fed from the second clock generator driven by a 33.33 MHz clock oscillator. SDRAM is clocked with 66.66 MHz.

3.1.2. SDRAM stage

The SDRAM (up to 128 MByte on-board) has its own DRAM bus containing memory addresses MA0..12, memory data MD0..31 and control signals for up to four banks. Due to small load no buffering of clocks and signals is necessary.

3.1.3. ROM stage

ROM or FLASH are driven by the general purpose address bus GPA0..25. It has three programmable chip selects with each up to 64 MByte range. The ROM Data bus is either the 32 bit general purpose bus GPD0..31 or the memory data bus MD0..31. Configuration pins decide, which bus at boot time is used. The bus size is selectable with 8, 16 or 32 bit. The MOD520C has a FLASH IC for up to 16 MByte 16 bit ROM or FLASH selected by BOOTCS# connected to MD0..15.

3.1.4. SRAM stage

The SRAM (512 KByte on-board) is buffered by VBAT. The Memory Location is defined in the System BIOS. ROMCS1# is used to access the SRAM.

3.1.5. 32 I/O Ports

The ÉlanSC520 CPU has 32 I/O ports. They have alternate functions. Most of them are control signals for GP bus (PIO0..26) used as ISA-bus. PIO27 (GPCS0#) is used as a programmable external chip select and PIO28,29 are not connected. PIO30,31 are used to drive a serial parameter EEPROM on-board.

3.1.6. 256 Byte EEPROM for BIOS and Applications on PIO30,31

An on-board serial EEPROM with 256 byte and I2C bus is controlled by PIO30 (I2CDAT) and PIO31 (I2CCLK). 128 byte are used for non-volatile BIOS defaults, the remaining range may contain application specific data and parameters. The BIOS contains calls to read and write to this memory (see BIOS documentation).

3.1.7. On-board Power Supply

The 2.5V on-board voltage is generated from +5V.

An external battery may be connected to the signal VBATIN. Battery status is controlled by BBATSEN, which sets a power fail bit in a status register for RTC, if BBATSEN is low at power-up.

3.1.8. Voltage Supervision, RESET Generation

Three voltages are used on board: +2.5V, +3.3V and +5V. U2 controls +5V and U10 controls +3.3V. LBOUT or PWRGOOD will become low, if these voltages are out of tolerance. An external SRESET# is wired or-ed to U10. It can also be activated from extended JTAG signal SRESET# via X1. The wired OR of 1RESET# and 2RESET# control U10. Its output PWRGOOD is low (not active), if either the signals described above from U10 are low or +5V is out of tolerance. Typical length of PWRGOOD low is longer than 1 sec (minimum 790 msec).

3.1.9. Serial Ports

The AMD ÉlanSC520 CPU has two internal asynchronous ports and one synchronous serial port. Both of this ports are available at the System Connectors.

3.1.10. Fast Ethernet Controller Stage

Connected to the PCI bus device 0 (REQ/GNT0#) of the Élan SC520 CPU, a Fast Ethernet Controller U7 supports 10/100Mbps transfer depending on driver software. X3 is a JST B5B-PH-SM3 5 pin connector. Parameters as physical address and power down modes are stored in a 64X16 bit Serial EEPROM controlled by U7. 2 status LEDs LE1, LE2 show the state of the Ethernet connection. For a more detailed hardware and software description see Intel 82559ER manual.

3.1.11. Dual CAN Controller Stage

The CAN Controller is selected via ROMCS1# and the Memory location is selectable in the BIOS Setup Screen. The CAN Interrupt provided by 82C900 is inverted by the onboard Lattice CPLD. Since the Interrupt asserted by the 82C900 is only a low active pulse of 0.2µs the CPLD holds the interrupt active until the software accesses the Memory at the location CAN-Base+1xxh. The BIOS routes this interrupt to IRQ11.

3.1.12. GP Bus used for ISA Bus

The AMD ÉlanSC520 CPU contains an 8/16bit General Purpose Bus (GP bus) with 26 address lines (GPA0..25), 16 data lines (GPD0..15) and different control lines using PIO ports in their alternate GP bus function. Its timing is programmable for speeds up to 33MHz. This bus is to emulate a 16 bit ISA bus (PC/104) running with 8 MHz. ISA bus signal are connected without buffers directly to the lines of the CPU due to the 5V tolerance of the 3.3V signals.

8 bit signals SMEMRD# and SMEMWR# (active only at addresses beyond 1 MByte) are not supported (GPMEM_RD# and GPMEM_WR# used).

The AMD ÉlanSC520 CPU has only 4 DMA channels on GP bus. DMA channel 2 is used for Super-I/O (U2) on EVAMOD520. All four channels are connected to edge connector X2.

Not supported ISA bus signals 0WS#, IOCHK#, IRQ15, REFRESH#, 8MHz and 14.318 MHz clocks, MASTER#.

4. Connectors Of MOD520C

4.1. System Connector X2

Pin	Function	I/O	Pin	Function	I/O
1	+3.3V	power	2	GND	power
3	+3.3V	power	4	GND	power
5	GPD0	I/O	6	TDP	O
7	GPD1	I/O	8	TDN	O
9	GPD2	I/O	10	not connected	
11	GPD3	I/O	12	RDP	I
13	GPD4	I/O	14	RDN	I
15	GPD5	I/O	16	not connected	
17	GPD6	I/O	18	DRQ0	I
19	GPD7	I/O	20	DRQ2	I
21	GPD8	I/O	22	DRQ5	I
23	GPD9	I/O	24	DRQ7	I
25	GPD10	I/O	26	DACK0#	O
27	GPD11	I/O	28	DACK2#	O
29	GPD12	I/O	30	DACK5#	O
31	GPD13	I/O	32	DACK7#	O
33	GPD14	I/O	34	GND	power
35	GPD15	I/O	36	GPRESET	O
37	GND	power	38	GPIORD#	O
39	GPA0	O	40	GPIOWR#	O
41	GPA1	O	42	GPALE	O
43	GPA2	O	44	GPBHE#	O
45	GPA3	O	46	GPRDY	I
47	GPA4	O	48	GPAEN	O
49	GPA5	O	50	GPTC	O
51	GPA6	O	52	GPDBUFOE#	O
53	GPA7	O	54	GPIO_CS16#	O
55	GPA8	O	56	GPMEM_CS16#	O
57	GPA9	O	58	GPCS0#	O
59	GPA10	O	60	GPMEM_RD#	O
61	GPA11	O	62	GPMEM_WR#	O
63	GPA12	O	64	GND	power

Pin	Function	I/O	Pin	Function	I/O
65	GPA13	O	66	EXTRES#	I
67	GPA14	O	68	PWRGOOD	O
69	BUFA15	O	70	CLKTEST	
71	BUFA16	O	72	PRG_RESET	
73	BUFA17	O	74	GND	power
75	BUFA18	O	76	GPCS1#	O
77	BUFA19	O	78	GPCS2#	O
79	BUFA20	O	80	GPCS3#	O
81	BUFA21	O	82	GPCS4#	O
83	BUFA22	O	84	GPCS5#	O
85	BUFA23	O	86	GPCS6#	O
87	BUFA24	O	88	GPCS7#	O
89	BUFA25	O	90	VBATIN	power
91	GND	power	92	GND	power
93	IRQ1	I	94	RSTLD0	I
95	IRQ3	I	96	RSTLD1	I
97	IRQ4	I	98	RSTLD2	I
99	IRQ5	I	100	RSTLD3	I
101	IRQ6	I	102	RSTLD4	I
103	IRQ7	I	104	RSTLD5	I
105	IRQ9	I	106	RSTLD6	I
107	IRQ10	I	108	RSTLD7	I
109	CANINT	I	110	DBGDIS	I
111	IRQ12	I	112	INSTRC	I
113	IRQ14	I	114	DBGENTR	I
115	SPEAKER	O	116	not connected	
117	+5V	power	118	GND	power
119	+5V	power	120	GND	power

4.2. System Connector X4

Pin	Function	I/O	Pin	Function	I/O
1	PCICLKRTN	I	2	GND	power
3	PCICLK	O	4	PCICLKETHER	I
5	AD0	I/O	6	CBE0#	I/O
7	AD1	I/O	8	CBE1#	I/O
9	AD2	I/O	10	CBE2#	I/O
11	AD3	I/O	12	CBE3#	I/O
13	AD4	I/O	14	not connected	
15	AD5	I/O	16	not connected	
17	AD6	I/O	18	not connected	
19	AD7	I/O	20	not connected	
21	AD8	I/O	22	GND	power
23	AD9	I/O	24	RXD1	I
25	AD10	I/O	26	TXD1	O
27	AD11	I/O	28	CTS1#	I
29	AD12	I/O	30	DCD1#	I
31	AD13	I/O	32	DSR1#	I
33	AD14	I/O	34	RIN1#	I
35	AD15	I/O	36	DTR1#	O
37	AD16	I/O	38	RTS1#	O
39	AD17	I/O	40	RXD2	I
41	AD18	I/O	42	TXD2	O
43	AD19	I/O	44	CTS2#	I
45	AD20	I/O	46	DCD2#	I
47	AD21	I/O	48	DSR2#	I
49	AD22	I/O	50	RIN2#	I
51	AD23	I/O	52	DTR2#	O
53	AD24	I/O	54	RTS2#	O
55	AD25	I/O	56	CANH1/TXD1	
57	AD26	I/O	58	CANL1/RXD1	
59	AD27	I/O	60	CANH2/TXD2	
61	AD28	I/O	62	CANL2/RXD2	
63	AD29	I/O	64	GND	power

Pin	Function	I/O	Pin	Function	I/O
65	AD30	I/O	66	SRESET#	I
67	AD31	I/O	68	GPRESET#	O
69	GND	power	70	TCK	O
71	INTA#	I	72	TMS	
73	INTB#	I	74	TDI	I
75	INTC#	I	76	TDO	O
77	INTD#	I	78	TRST#	I
79	REQ0#	I	80	CMDACK	
81	REQ1#	I	82	BR/TC	
83	REQ2#	I	84	GND	Power
85	REQ3#	I	86	STOP/TX	
87	REQ4#	I	88	TRIG/TRACE	
89	GNT0#	O	90	not connected	
91	GNT1#	O	92	ACTLED#	O
93	GNT2#	O	94	LILED#	O
95	GNT3#	O	96	SPEEDLED#	O
97	GNT4#	O	98	not connected	
99	GND	power	100	GND	power
101	PAR	I/O	102	SSI_CLK	O
103	PERR#	I/O	104	SSI_DO	O
105	SERR#	I	106	SSI_DI	I
107	FRAME#	I/O	108	not connected	
109	TRDY#	I/O	110	ISP_TDI	I
111	IRDY#	I/O	112	ISP_TDO	O
113	STOP#	I/O	114	ISP_TMS	
115	DEVSEL#	I/O	116	ISP_TCK	I
117	RST#	O	118	BSCAN#	
119	GND	power	120	GND	power

5. Application Notes

5.1. Power Supply

The MOD520C needs +3.3V and 5V power supply.

3.3V worst case supply current is 1130 mA

5V worst case supply current is 550 mA

Be sure to design your power supply for this current including large load transients.

5.2. Important Signals

5.2.13. PCICLKRTN PCICLK PCICLKETHER

PCICLK is the clock source for the PCI-Bus. PCICLKETHER is the clock input for the Ethernet Controller. PCICLKRTN is the clock input of the AMD Élan Sc520. This pin is used to synchronize the CPU with the external PCI-Bus. Therefore it is important that all clock traces have the same length to provide each PCI-Target with the clock at the same time. Trace length of each of this clocks is 68mm on the module. If you do not plan to connect an additional PCI-Target on your board you just add a serial resistor 33R between PCICLK and PCICLKRTN and one between PCICLK and PCICLKETHER.

5.2.14. ISA-Bus Signals

If you use the ISA-Bus Signals you have to add some resistors to the following Signals:

GPD0 – GPD15	4k7 pull up
GPRDY	1k pull down
IRQ´s	10k pull up
DRQ´s	10k pull down

5.2.15. CAN-Interrupt IRQ11

IRQ11 is used for the CAN-Controller 82C900 and is not sharable. Since the interrupt provided by 82C900 is a low active pulse with a length of 0.2µs the CPLD inverts this signal and holds it until the software acknowledges the interrupt. To acknowledge this interrupt the software has to access a memory location with the offset 1xxh to the CAN-Base. This memory access is just an access of the system memory, not an access of the CAN-Controller.

6. Members of the MOD520C family

Number	Variant	Flash	SDRAM	SRAM	CAN	CAN-Driver	Temp.
320	MOD520C_0_V01	8M*16, Strata (=**16 Mbyte**) 1*TM01445	2*4M*16 (=**16 Mbyte**) 2*TM01519	512k*8	Yes	Yes	0..70°
321	MOD520C_0_V02	1M*16, AMD (=**2 Mbyte**) 1*TM01520	2*4M*16 (=**16 Mbyte**) 2*TM01519	512k*8	Yes	Yes	0..70°
322	MOD520C_0_V03	8M*16, Strata (=**16 Mbyte**) 1*TM01445	2*16M*16 (=**64 Mbyte**) 2*TM01249	512k*8	Yes	Yes	0..70°
334	MOD520C_1_V01 MOD520C_2_V01	8M*16, Strata (=**16 Mbyte**) 1*TM01445	2*4M*16 (=**16 Mbyte**) 2*TM01519	512k*8 TM0	Yes	no	0..70°
335	MOD520C_1_V02 MOD520C_2_V02	1M*16, AMD (=**2 Mbyte**) 1*TM01520	2*4M*16 (=**16 Mbyte**) 2*TM01519	512k*8 TM0	Yes	no	0..70°
336	MOD520C_1_V03 MOD520C_2_V03	8M*16, Strata (=**16 Mbyte**) 1*TM01445	2*16M*16 (=**64 Mbyte**) 2*TM01249	512k*8 TM0	Yes	no	0..70°
184	MOD520C_1_V04	8M*16, Strata (=**16 Mbyte**) 1*TM01445	2*4M*16 (=**16 Mbyte**) 2*TM01519	No	No	No	0..70°