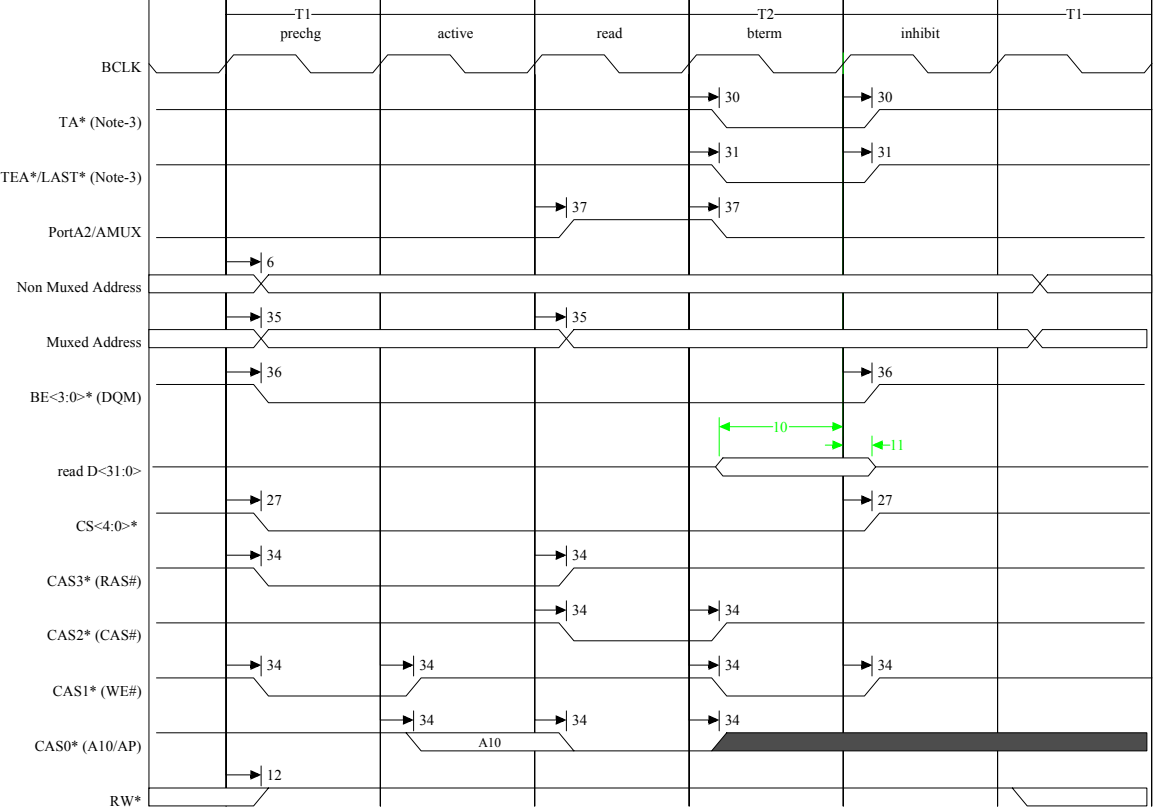

Note-1 Port Size determines which Byte Enable signals are active.
8-bit port = BE3*, 16-bit port = BE[3:2], 32-bit port = BE[3:0]

Note-2 The Precharge and/or the Active commands are not always present. They depend on the address of the previous SDRAM access.

Note-3 The TA* and TEA*/LAST signals are for reference only.

SD_RD_caslat1.td SDRAM Read, Cas Latency = 1