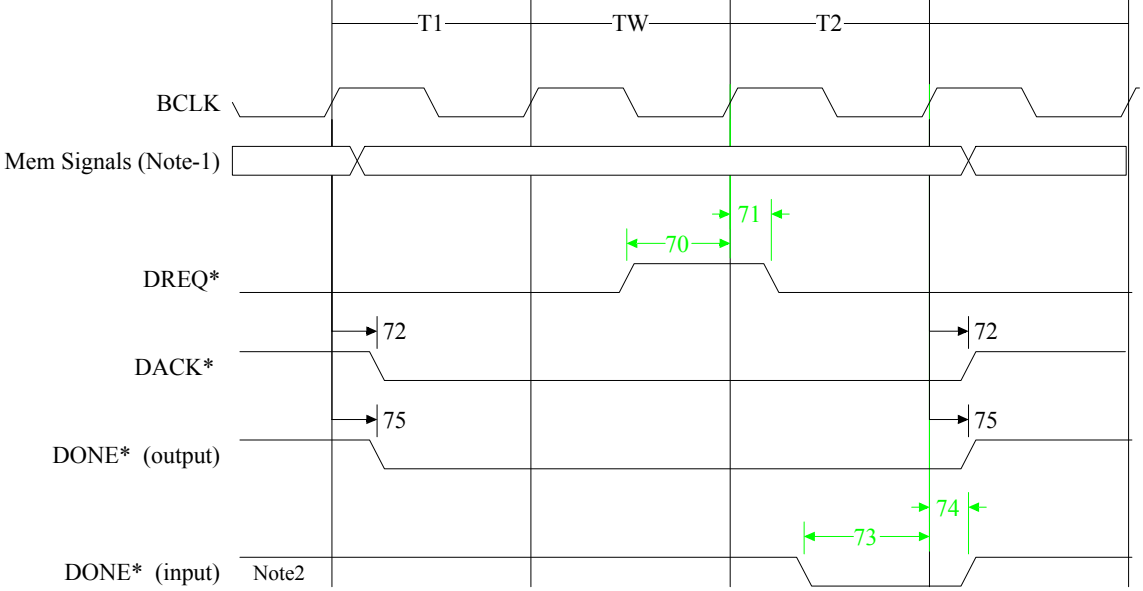

Note-1 The Memory Signals consist of Data[31:0], Addr[27:0], BE[3:0], CS/RAS[4:0] CAS[3:0], RW, OE*, WE*, PortC3/AMUX. The timing of these signals depends on how the memory is configured (Sync SRAM, Async SRAM, FP DRAM, or SDRAM).

Note-2 The DONE* signal will work as an input only when the DMA Channel is configured as Fly-By Write.

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