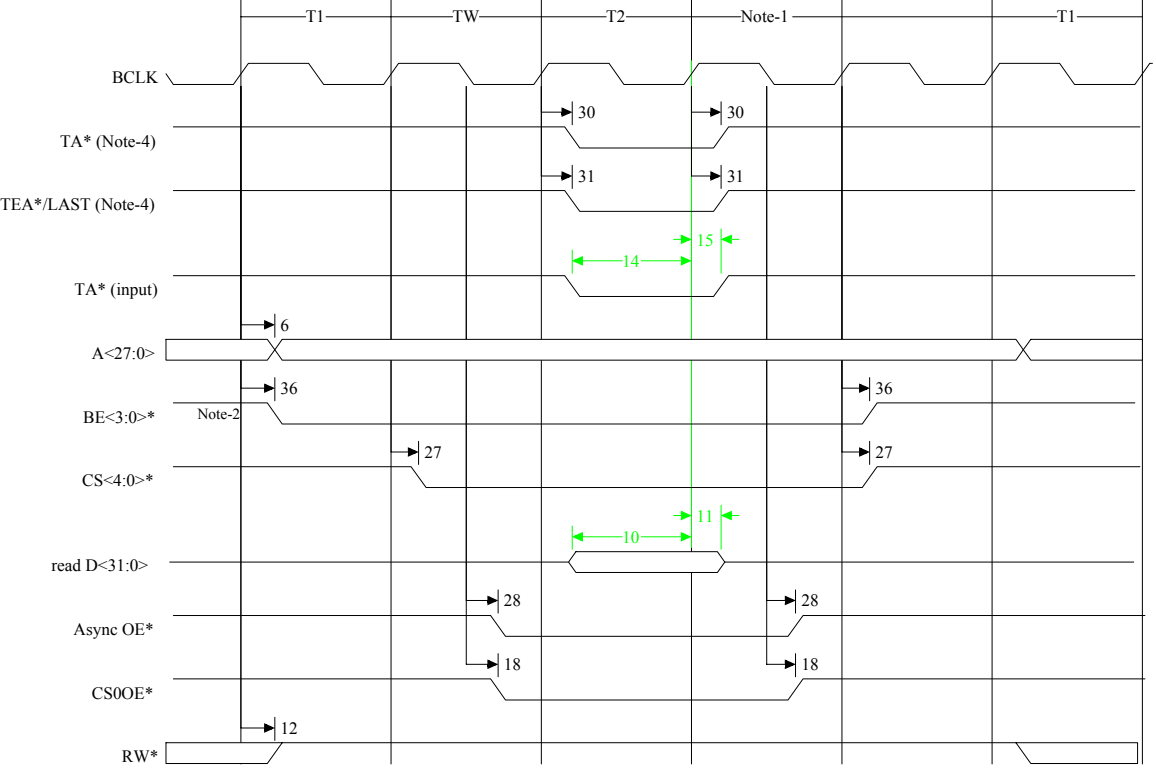


Note-1 There is always at least null one period between memory transfers. There can be more null periods if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.
Note-2 Port Size determines which Byte Enable signals are active.
8-bit port = BE3*, 16-bit port = BE[3:0], 32-bit port = BE[3:0]
Note-3 The TW cycles are present when the WAIT field is set to 2 or more.
Note-4 The TA* and TEA*/LAST signals are for reference only.

Sram_OE_RD.TD - OE* Controlled Read, (Wait = 2)