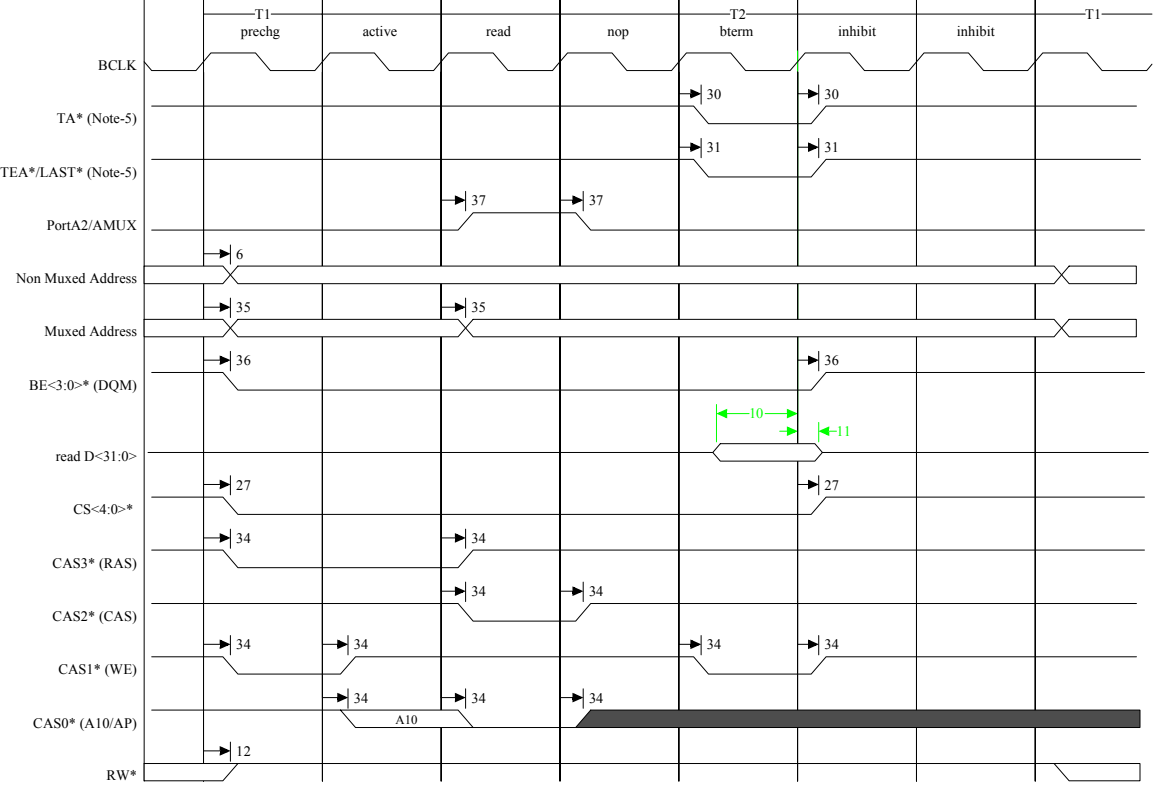


Note-1 Port Size determines which Byte Enable signals are active.
8-bit port = BE3*, 16-bit port = BE[3:2], 32-bit port = BE[3:0]
Note-2 The Precharge and/or the Active commands are not always present. They depend on the address of the previous SDRAM access.
Note-3 If CAS Latency = 3 then there are 2 NOPs between the Read and Burst Terminate Commands
Note-4 If CAS Latency = 3 then there are 3 Inhibits after Burst Terminate.
Note-5 The TA* and TEA*/LAST signals are for reference only.

SD_RD.td SDRAM Read, Cas Latency = 2