

## SDRAM INTERFACE TIMING CHARACTERISTICS

BCLK max frequency 55.296MHz

Operating conditions:

TEMPERATURE: -15.00 (min) 110.00 (max)

VOLTAGE : 1.60 (min) 1.40 (max)

OUTPUT LOAD : 25.0pf

INPUT DRIVE : CMOS BUFFER

Num	Characteristic	Min	Max	Unit
12	BCLK high to RW <sub> </sub> valid		13.5	ns
36	BCLK high to BE <sub> </sub> /QDM <sub> </sub> valid		15.5	ns
6	BCLK high to Non Muxed Address valid	5	13.5	ns
9	BCLK high to Data Out valid		14	ns
13	BCLK high to Data Out high impedance		13	ns
10	Data in valid to BCLK high (setup)	5		ns
11	BCLK high to Data in invalid (hold)	0		ns
27	BCLK high to CS* <sub> </sub> valid		15.5	ns
30	BCLK high to TA <sub> </sub> valid		13.5	ns
31	BCLK high to TEA <sub> </sub> valid		16	ns
37	BCLK high to PORTA2/AMUX valid		14	ns
35	BCLK high to Muxed Address valid	6	14.5	ns
34	BCLK high to CAS* <sub> </sub> valid		12	ns

Figure 1. SDRAM Interface Timing Characteristics

Note: Parameter 11 was changed from 3ns to 0ns based on additional characterization.