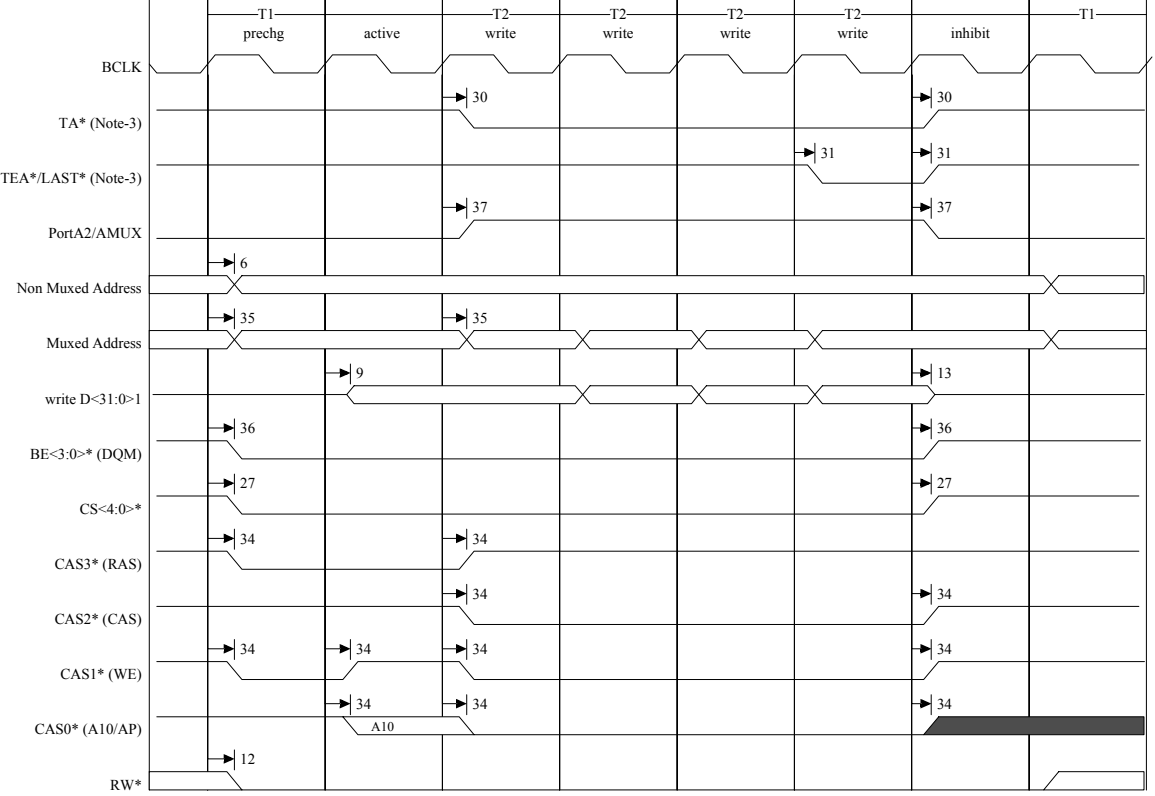

Note-1 Port Size determines which Byte Enable signals are active.
8-bit port = BE3*, 16-bit port = BE[3:2], 32-bit port = BE[3:0]

Note-2 The Precharge and/or the Active commands are not always present. They depend on the address of the previous SDRAM access. When the Active command is not present, Perameter #35 is valid during the Write (T2) cycle.

Note-3 The TA* and TEA*/LAST signals are for reference only.

SD_brWR.td SDRAM Burst Write