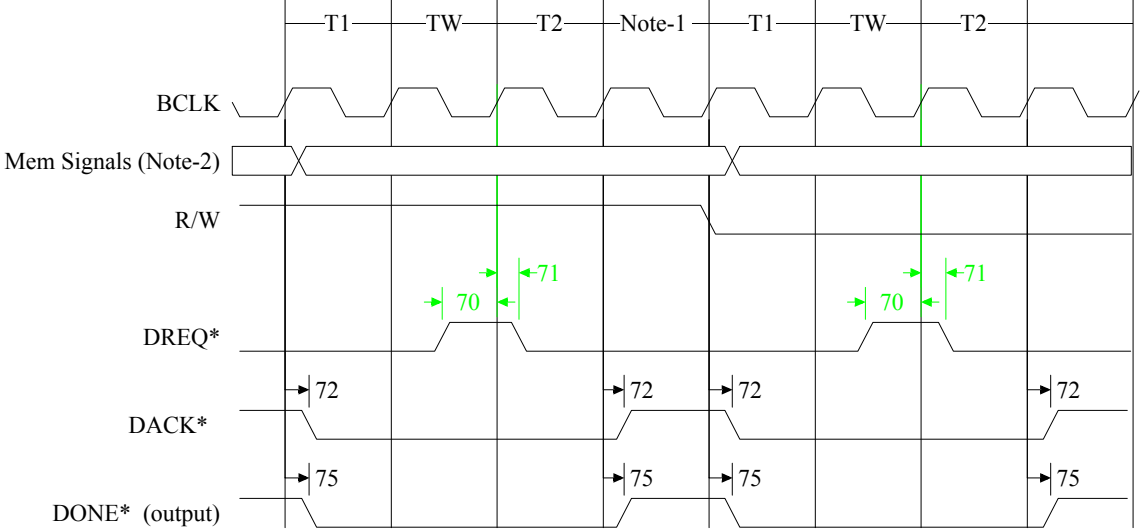

Note-1 There is sometimes a null period between memory cycles.
Note-2 The Memory Signals consist of Data[31:0], Addr[27:0], BE[3:0], CS/RAS[4:0], CAS[3:0], RW, OE*, WE*, PortA2/AMUX. The timing of these signals depends on how the memory is configured (Sync SRAM, Async SRAM, FP DRAM, or SDRAM).

MEM_to_MEM_Ext_DMA.TD