



Note-1 There can be null periods between memory transfers if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

Note-2 Port Size determines which Byte Enable signals are active.
8-bit port = BE3*, 16-bit port = BE[3:2], 32-bit port = BE[3:0]

Note-3 Port Size determines which CAS signals are active.
8-bit port = CAS3*, 16-bit port = CAS[3:2], 32-bit port = CAS[3:0]

Note-4 The TA* and TEA*/LAST signals are for reference only.