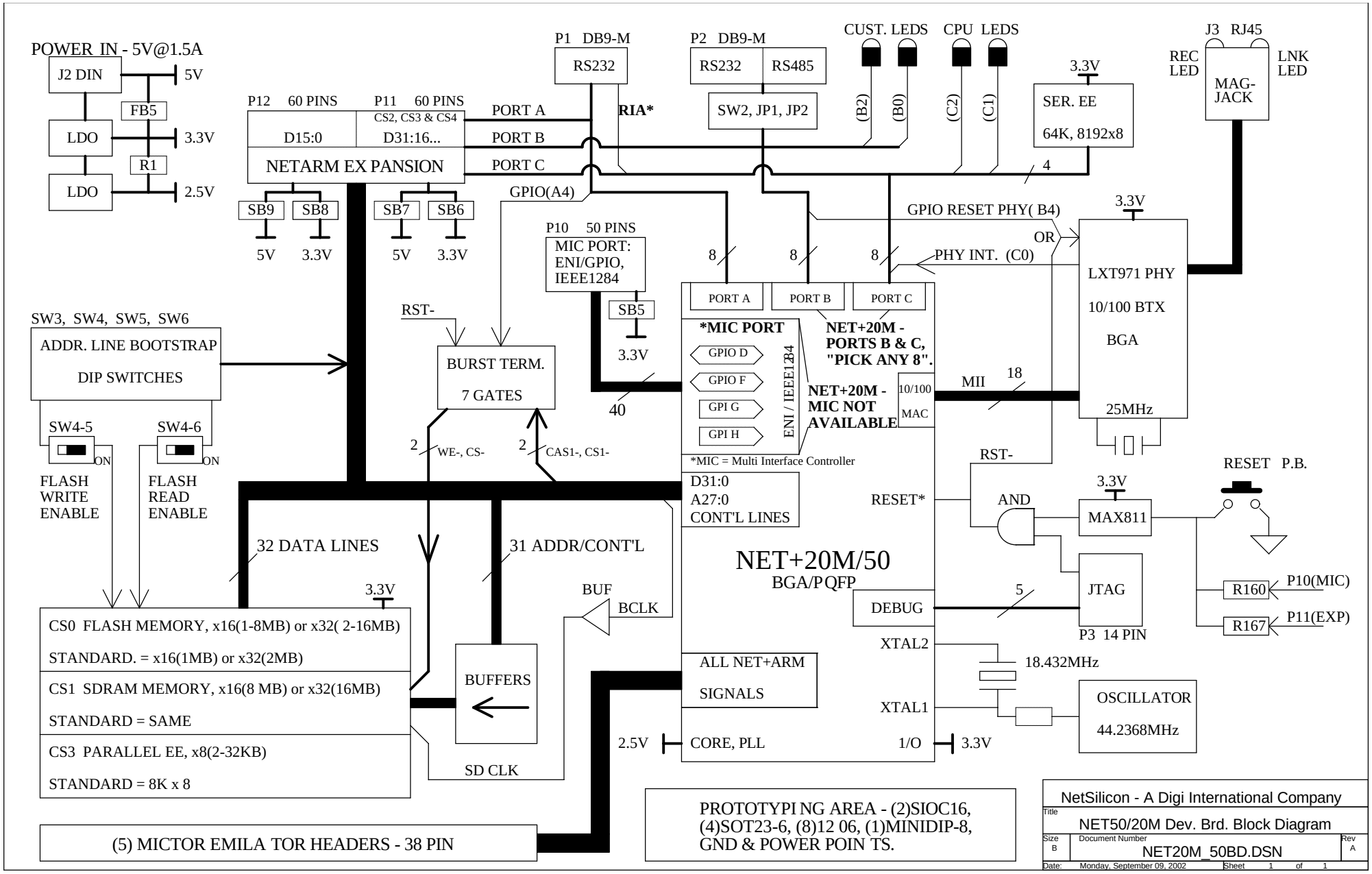
POWER IN - 5V@1.5A
J2 DIN
5V
FB5
LDO
3.3V
R1
LDO
2.5V
P12 60 PINS
P11 60 PINS
CS2, CS3 & CS4
D15:0
D31:16...
NETARM EX PANSION
PORT A
PORT B
PORT C
SB9
SB8
SB7
SB6
5V
3.3V
5V
3.3V
P1 DB9-M
RS232
RIA*
P2 DB9-M
RS232
RS485
SW2, JP1, JP2
CUST. LEDS
CPU LEDS
(B2)
(B0)
(C2)
(C1)
3.3V
SER. EE
64K, 8192x8
4
J3 RJ45
REC LED
LNK LED
MAG-JACK
GPIO(A4)
GPIO RESET PHY(B4)
OR
PHY INT. (C0)
3.3V
LXT971 PHY
10/100 BTX
BGA
25MHz
P10 50 PINS
MIC PORT:
ENI/GPIO,
IEEE1284
SB5
3.3V
40
8
8
8
PORT A
PORT B
PORT C
*MIC PORT
GPIO D
GPIO F
GPI G
GPI H
ENI / IEEE1284
NET+20M - PORTS B & C, "PICK ANY 8".
NET+20M - MIC NOT AVAILABLE
10/100 MAC
MII
18
*MIC = Multi Interface Controller
SW3, SW4, SW5, SW6
ADDR. LINE BOOTSTRAP
DIP SWITCHES
RST-
BURST TERM.
7 GATES
SW4-5
SW4-6
ON
ON
FLASH WRITE ENABLE
FLASH READ ENABLE
2
WE-, CS-
2
CAS1-, CS1-
D31:0
A27:0
CONT'L LINES
RESET*
RST-
AND
3.3V
MAX811
RESET P.B.
32 DATA LINES
31 ADDR/CONT'L
NET+20M/50
BGA/PQFP
3.3V
BUF
BCLK
DEBUG
5
JTAG
P3 14 PIN
R160
P10(MIC)
R167
P11(EXP)
CS0 FLASH MEMORY, x16(1-8MB) or x32(2-16MB)
STANDARD. = x16(1MB) or x32(2MB)
CS1 SDRAM MEMORY, x16(8 MB) or x32(16MB)
STANDARD = SAME
CS3 PARALLEL EE, x8(2-32KB)
STANDARD = 8K x 8
BUFFERS
SD CLK
ALL NET+ARM
SIGNALS
XTAL2
18.432MHz
XTAL1
OSCILLATOR
44.2368MHz
2.5V
CORE, PLL
1/O
3.3V
(5) MICTOR EMILA TOR HEADERS - 38 PIN
PROTOTYPI NG AREA - (2)SIOC16, (4)SOT23-6, (8)12 06, (1)MINIDIP-8, GND & POWER POIN TS.
NetSilicon - A Digi International Company
Title
NET50/20M Dev. Brd. Block Diagram
Size B
Document Number
NET20M_50BD.DSN
Rev A
Date: Monday, September 09, 2002
Sheet 1 of 1