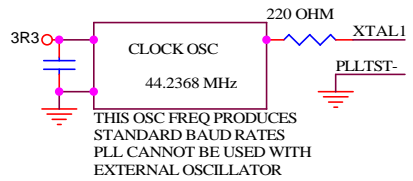


SYSTEM DATA BUS

SYSTEM ADDRESS BUS SEE NOTE 1

OPTIONAL OSCILLATOR SEE NOTE 5

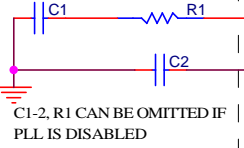


X16 FLASH BOOT

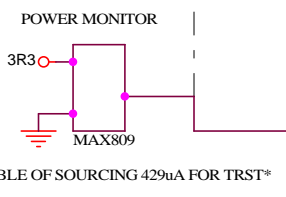
A DISABLE OF FLASH IS RECOMMENDED



NETARM	C1	C2	R1
12-40	.01	.001(OMIT)	100
50-1	.47	.047	100
50-3	.015	.0015	820

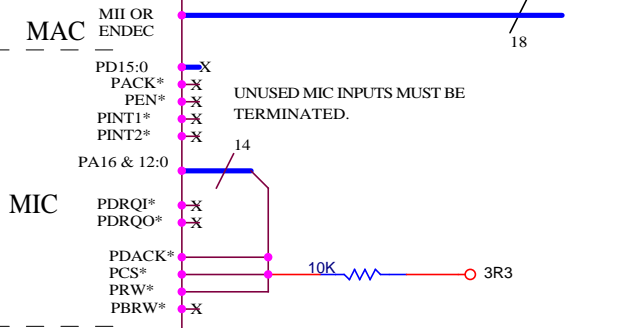


REFER TO LATEST DEBUGGER APP NOTES:
BASIC PRODUCTION CIRCUIT HAS TRST* TIED TO RESET*, NO CONNECTIONS TO DEBUGGER CONNECTOR PINS 3 & 12.



NET+50-3

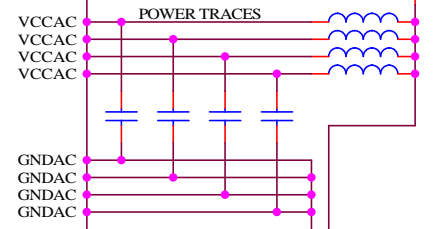
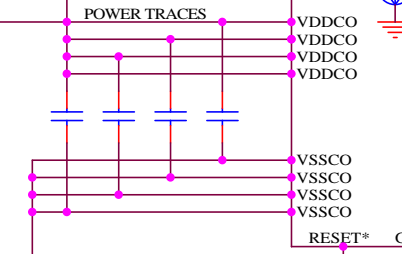
TO 10/100 ETHERNET DEVICES



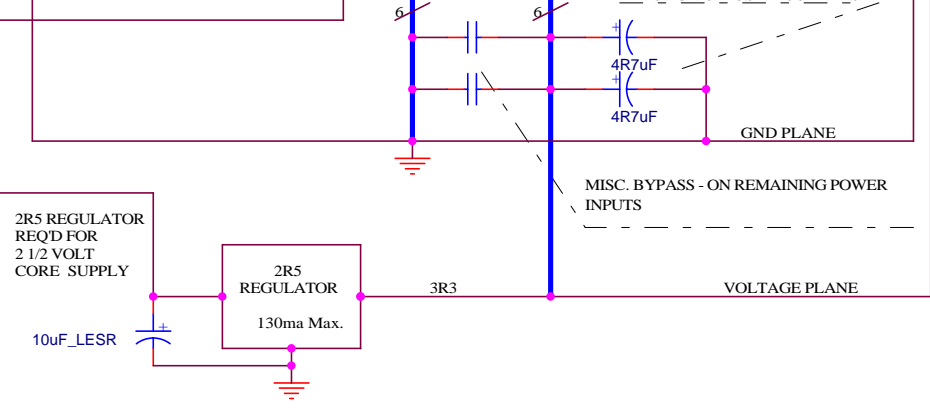
A SERIAL MONITOR IS RECOMMENDED FOR DEBUG. MINIMUM REQUIREMENT = TXD, RXD, & GND TO A HEADER.

CHIP SELECTS TO MEMORY AND I/O DEVICES

NOT USED IF A26 & A27 SET FOR CS0OE* CS0WE*
IF EXTERNAL CLOCK IS REQUIRED, PLACE A 15-22 OHM RESISTOR IN SERIES WITH BCLK LOCATED NEAR PIN.



BEADS 80-200Z; 200ma MINIMUM.



NOTES:

- 1) ADDRESS LINES CAN BE USED FOR POWERUP CONFIGURATION. 1K PULL-DOWNS ARE REQUIRED TO OVERCOME THE INTERNAL 352uA CURRENT SOURCES.
- 2) THE 510 OHM PULL-UPS ARE REQUIRED ON TA* & TEA* BECAUSE THE INTERNAL BUS MASTER DOES NOT DRIVE THESE SIGNALS POSITIVE BEFORE TRI-STATING. THE LOW VALUE EXTERNAL RESISTOR PRODUCES A FASTER SIGNAL RISE TIME.
- 3) 3R3, 2R5, & 4R7; R = DECIMAL POINT.
- 4) ALL UNMARKED CAPACITORS ARE 100nF
- 5) TO USE EXTERNAL OSCILLATOR, PULL PLLTST* TO A LOGIC "0". THIS BYPASSES THE PLL; XTAL1 = SYSCCLK. SEE "OPTIONAL OSCILLATOR" DRAWING ABOVE.
- 6) FERRITE BEAD "FB1" TO PLLVDD CAN BE BYPASSES IF PLL IS DISABLED.