EVANET

User's Manual

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Board Revision EVANET_1

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1. General

EVANET_1 is the standard base board for modules using NetSilicon's NET+ARM microcontrollers, such as the ModNET50.

2. Features

- 4-layer PCB
- 5V power supply
- Power LED
- 3.3V regulator for module's main power supply
- Connectors for the module
- One serial interface RS232, COM A, with all handshaking signals on 9-pin SUBD male connector
- One serial interface RS232, COM B, without handshaking signals on 9-pin SUBD male connector
- Transformer for the Ethernet.
- RJ45 jack for Ethernet interface
- 2 LEDs for Ethernet (Link/Activity, 10/100Mbit).
- 1 Debug LED
- Configuration switches (7 bits). These switches are latched at end of reset to bit field GEN_ID[4-10] in the NET+ARM's System Status Register.
- Dip switch to select between little-endian and big-endian
- Jumper to disable Flash memory

- One 9-pin SUBD male connector for the 1st CAN channel. The 2nd CAN channel is available on a 10-pin header.
- Battery for backup of RTC and SRAM
- JTAG connector, Berg 14-pin, dual row 2.54 mm, ARM standard
- JTAG connector, 8-pin single row, 2.54mm, for FS Forth-Systeme's JTAG Booster
- Multi-ICE connector 20-pin dual row 2.54mm
- CompactFlash card holder with ejector
- Pulse generator which generates a square-wave signal between 1300Hz and 14kHz
- USB ports for host interface (A-type connector) and device interface (B-type connector) for future derivatives of the NetSilicon chips.
- Reset push button
- 4 user-definable push buttons
- 4 user-definable LEDs
- buzzer
- optional graphic controller adaptable

3. Module Pins

3.1. System Connector X2

Pin X2-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
-	CS5#	-	-	O	-	Reserved
-	CS6#	-	-	O	-	Reserved
-	CS7#	-	-	O	-	Reserved
1	GND	-	-	P	-	
2	GND	-	-	P	-	
3	GND	-	-	P	-	
4	GND	-	-	P	-	
5	LITEND#	-	-	I	No	Low -> Little-Endian, not available on module ModNET50_0
6	CSMODE	-	-	I	Yes	High -> CS3# and CS4# available for external use Low -> CS4# only available for external use This signal is not available on modules ModNET50_0 and ModNET50_1
7	A0	-	-	O	Yes	Address Bus
9	A1	-	-	O	Yes	Address Bus
11	A2	-	-	O	Yes	Address Bus
13	A3	-	-	O	Yes	Address Bus
15	A4	-	-	O	Yes	Address Bus
17	A5	-	-	O	Yes	Address Bus
19	A6	-	-	O	Yes	Address Bus
21	A7	-	-	O	Yes	Address Bus
23	A8	-	-	O	Yes	Address Bus
25	A9	-	-	O	Yes	Address Bus
27	A10	-	-	O	Yes	Address Bus
29	A11	-	-	O	Yes	Address Bus
31	A12	-	-	O	Yes	Address Bus
33	A13	-	-	O	Yes	Address Bus
35	A14	-	-	O	Yes	Address Bus
36	CFG4	-	-	I	No	Connected to A13, = System Status Register Bit 4
37	A15	-	-	O	Yes	Address Bus
38	CFG5	-	-	I	No	Connected to A14, = System Status Register Bit 5
39	RSTIN#	-	-	I	No	Reset input

Pin X2-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
40	CFG6	-	-	I	No	Connected to A15, = System Status Register Bit 6
41	PWRGOOD	-	-	O	No	Output of the reset controller
42	CFG7	-	-	I	No	Connected to A16, = System Status Register Bit 7
43	GND	-	-	P	-	
44	GND	-	-	P	-	
45	A16	-	-	O	Yes	Address Bus
47	A17	-	-	O	Yes	Address Bus
49	A18	-	-	O	Yes	Address Bus
51	A19	-	-	O	Yes	Address Bus
54	TRST#	-	-	I	No	JTAG, not available on module ModNET50_0
56	TCK	-	-	I	No	JTAG, not available on module ModNET50_0
58	TMS	-	-	I	No	JTAG, not available on module ModNET50_0
60	TDI	-	-	I	No	JTAG, not available on module ModNET50_0
61	WE#	-	-	O	Yes	
62	TDO	-	-	O	No	JTAG, not available on module ModNET50_0
63	OE#	-	-	O	Yes	
64	FLSH_DIS	-	-	I	No	Disable Flash on module. Needed to enter debugger, if Flash is empty. Not available on module ModNET50_0
65	R/W#	-	-	O	Yes	
66	TS#	-	-	O	No	Transfer Start, not available on module ModNET_0
67	BCLK	-	-	O	Yes	System Clock
68	TA#	-	-	O	No	Data Transfer Acknowledge
69	CS3#	-	-	O	Yes	External chip select, see signal CSMODE
70	TEA#	TLAST#	-	O	No	Data Transfer Error Acknowledge
71	CS4#	-	-	O	Yes	External chip select, see signal CSMODE
72	BG#	-	-	I/O	No	Bus Grant
73	BE2#	-	-	O	Yes	
74	BR#	-	-	I/O	No	Bus Request
75	BE3#	-	-	O	Yes	
76	BUSY#	-	-	I/O	No	Bus Busy

Pin X2-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
77	GND	-	-	P	-	
79	CS2#	-	-	O	Yes	Used on the module to select SRAM and CAN, see signal CSMODE
80	CFG8	-	-	I	No	Connected to A17, = System Status Register Bit 8
81	D16	-	-	I/O	Yes	Data Bus
82	CFG9	-	-	I	No	Connected to A18, = System Status Register Bit 9
83	D17	-	-	I/O	Yes	Data Bus
84	CFG10	-	-	I	No	Connected to A19, = System Status Register Bit 10
85	D18	-	-	I/O	Yes	Data Bus
87	D19	-	-	I/O	Yes	Data Bus
89	D20	-	-	I/O	Yes	Data Bus
91	D21	-	-	I/O	Yes	Data Bus
93	D22	-	-	I/O	Yes	Data Bus
95	D23	-	-	I/O	Yes	Data Bus
97	D24	-	-	I/O	Yes	Data Bus
99	D25	-	-	I/O	Yes	Data Bus
101	D26	-	-	I/O	Yes	Data Bus
103	D27	-	-	I/O	Yes	Data Bus
105	D28	-	-	I/O	Yes	Data Bus
107	D29	-	-	I/O	Yes	Data Bus
109	D30	-	-	I/O	Yes	Data Bus
111	D31	-	-	I/O	Yes	Data Bus
113	GND	-	-	P	-	
114	GND	-	-	P	-	
115	GND	-	-	P	-	
116	GND	-	-	P	-	
117	+3.3V	-	-	P	-	
118	+3.3V	-	-	P	-	
119	+3.3V	-	-	P	-	
120	+3.3V	-	-	P	-	

3.2. Peripheral Connector X3

Pin X3-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
1	GND	-	-	P	-	
2	GND	-	-	P	-	
3	+5V	-	-	P	-	
4	+5V	-	-	P	-	
5	PORTA0	DCDA#	DONE1#	I/O	No	COM A, DCD#
6	PORTA1	CTSA#		I/O	No	COM A, CTS#
7	PORTA2	DSRA#	DACK1#	I/O	No	COM A, DSR#
8	PORTA3	RXDA		I/O	No	COM A, RXD
9	PORTA4	RXCA#	OUT1A#	I/O	No	Debug LED
10	PORTA5	RTSA#		I/O	No	COM A, RTS#
11	PORTA6	DTRA#	DREQ1#	I/O	No	COM A, DTR#
12	PORTA7	TXDA		I/O	No	COM A, TXD
13	PORTB0	DCDB#	DONE2#	I/O	No	REG#/IOIS16#
14	PORTB1	CTSB#	RPSF#	I/O	No	
15	PORTB2	DSRB#	DACK2#	I/O	No	
16	PORTB3	RXDB		I/O	No	COM B, RXD
17	PORTB4	RXCB	OUT1B#	I/O	No	
18	PORTB5	RTSB#	REJECT#	I/O	No	
19	PORTB6	DTRB#	DREQ2#	I/O	No	
20	PORTB7	TXDB		I/O	No	COM B, TXD
21	PORTC0	CI0		I/O	No	ModNET50_0/ModNET50_1: Used as Interrupt Input from PHY ModNET50_2: Used for SDRAM reset bug fix
22	PORTC1	CI1		I/O	No	Used as Interrupt Input from RTC
23	PORTC2	CI2		I/O	No	Used as Interrupt Input from CAN
24	PORTC3	CI3	AMUX	I/O	No	Used as Interrupt Input from NE556 or CompactFlash
25	PORTC4	RIB#	RESET#	I/O	No	ModNET50_0: Reset Output to PHY and CAN-Controller ModNET50_1: Reset for CAN-Controller
26	PORTC5	TXCB	OUT2B#	I/O	No	ModNET50_0: I2CCLK, Used as I²C clock ModNET50_1: free
27	PORTC6	RIA#	IRQ#	I/O	No	ModNET50_0: Used for SDRAM reset bug fix ModNET50_1: I2CCLK, Used as I²C clock
28	PORTC7	TXCA	OUT2A#	I/O	No	I2CDAT, Used as I²C data
29	PORTD0			I/O	-	Reserved for NET+150

Pin X3-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
30	PORTD1			I/O	-	Reserved for NET+150
31	PORTD2			I/O	-	Reserved for NET+150
32	PORTD3			I/O	-	Reserved for NET+150
33	PORTD4			I/O	-	Reserved for NET+150
34	PORTD5			I/O	-	Reserved for NET+150
35	PORTD6			I/O	-	Reserved for NET+150
36	PORTD7			I/O	-	Reserved for NET+150
37	PORTE0			I/O	-	Reserved for NET+150
38	PORTE1			I/O	-	Reserved for NET+150
39	PORTE2			I/O	-	Reserved for NET+150
40	PORTE3			I/O	-	Reserved for NET+150
41	PORTE4			I/O	-	Reserved for NET+150
42	PORTE5			I/O	-	Reserved for NET+150
43	PORTE6			I/O	-	Reserved for NET+150
44	PORTE7			I/O	-	Reserved for NET+150
45	GND	-	-	P	-	
46	GND	-	-	P	-	
47	TPIP2	-	-	I	-	Reserved for NET+150, Ethernet 2 Input+
48	TPIP1	-	-	I	-	Ethernet 1 Input+
49	TPIN2	-	-	I	-	Reserved for NET+150, Ethernet 2 Input-
50	TPIN1	-	-	I	-	Ethernet 1 Input-
51	TPOP2	-	-	O	-	Reserved for NET+150, Ethernet 2 Output+
52	TPOP1	-	-	O	-	Ethernet 1 Output+
53	TPON2	-	-	O	-	Reserved for NET+150, Ethernet 2 Output-
54	TPON1	-	-	O	-	Ethernet 1 Output-
55	LEDLNK2	-	-	O	-	Reserved for NET+150, Ethernet 2 Line/Activity LED
56	LEDLNK1	-	-	O	-	Ethernet 1 Line/Activity LED
57	LEDH2	-	-	O	-	Reserved for NET+150, Ethernet 2 10/100 Mbit LED
58	LEDH1	-	-	O	-	Ethernet 1 10/100 Mbit LED
59	ESD2	-	-	I	-	Reserved for NET+150, Ethernet 2 Signal detect
60	ESD1	-	-	I	-	Ethernet 1 Signal detect
61	EVCC2	-	-	P	-	Reserved for NET+150, Ethernet 2 VCC, used for magnetics
62	EVCC1	-	-	P	-	Ethernet 1 VCC, used for magnetics

Pin X3-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
63	EGND2	-	-	P	-	Reserved for Ethernet 2 GND
64	EGND1	-	-	P	-	Ethernet 1 GND
65	PACK#	PCLKD1	GPIOF7	I/O	No	
66	CANH/TXDA	-	-	I/O	Yes	CAN_TXD or CANH, channel A
67	PEN#	PCLKD2	GPIOF6	I/O	No	
68	CANL/RXDA	-	-	I/O	Yes	CAN_RXD or CANL, channel A
69	PINT1#	PCLKD3	GPIOF5	I/O	No	
70	CANH/TXDB	-	-	I/O	Yes	CAN_TXD or CANH, channel B
71	PINT2#	PCLKD4	GPIOF4	I/O	No	
72	CANL/RXDB	-	-	I/O	Yes	CAN_RXD or CANL, channel B
73	GND	-	-	P	-	
74	GND	-	-	P	-	
75	PDATA0	-	GPIOD0	I/O	No	
76	PA0	ACK1#	GPIOH0	I/O	No	
77	PDATA1	-	GPIOD1	I/O	No	
78	PA1	ACK2#	GPIOH1	I/O	No	
79	PDATA2	-	GPIOD2	I/O	No	
80	PA2	ACK3#	GPIOH2	I/O	No	
81	PDATA3	-	GPIOD3	I/O	No	
82	PA3	ACK4#	GPIOH3	I/O	No	
83	PDATA4	-	GPIOD4	I/O	No	
84	PA4	BUSY1	GPIOH4	I/O	No	
85	PDATA5	-	GPIOD5	I/O	No	
86	PA5	BUSY2	GPIOH5	I/O	No	
87	PDATA6	-	GPIOD6	I/O	No	
88	PA6	BUSY3	GPIOH6	I/O	No	
89	PDATA7	-	GPIOD7	I/O	No	
90	PA7	BUSY4	GPIOH7	I/O	No	
91	PDATA8	POE1#	-		No	
92	PA8	PE1	GPIOG0	I/O	No	
93	PDATA9	POE2#	-		No	
94	PA9	PE2	GPIOG1	I/O	No	
95	PDATA10	POE3#	-		No	
96	PA10	PE3	GPIOG2	I/O	No	
97	PDATA11	POE4#	-		No	
98	PA11	PE4	GPIOG3	I/O	No	
99	PDATA12	PCLKC1#	-		No	
100	PA12	PSELECT1	GPIOG4	I/O	No	
101	PDATA13	PCLKC2#	-		No	
102	PA13	PSELECT2	GPIOF3	I/O	No	
103	PDATA14	PCLKC3#	-		No	

Pin X3-	Signal	2nd func. On NET+50	3rd func. On NET+50	Type	5V tol.	Description
104	PA14	PSELECT3	GPIOF2	I/O	No	
105	PDATA15	PCLKC4#	-		No	
106	PA15	PSELECT4	GPIOG5	I/O	No	
107	PCS#	FAULT2#	GPIOG7	I/O	No	
108	PA16	FAULT1#	GPIOG6	I/O	No	
109	PRW#	FAULT3#	GPIOF0	I/O	No	
110	USBP	-	-	I/O	-	Reserved for USB data +
111	PBRW#	FAULT4#	GPIOF1	I/O	No	
112	USBN	-	-	I/O	-	Reserved for USB data -
113	GND	-	-	P	-	
114	GND	-	-	P	-	
115	GND	-	-	P	-	
116	GND	-	-	P	-	
117	+3.3V	-	-	P	-	
118	VBAT	-	-	P	-	For backup of SRAM and RTC
119	+3.3V	-	-	P	-	
120	VBAT	-	-	P	-	For backup of SRAM and RTC

4. Detailed Description

4.1. JTAG Connector

There are three connectors to adapt to the JTAG interface of the NET+ARM CPUs: The 1st is the ARM standard 14-pin connector. The 2nd connector with 8 pins can be used to interface to the FS Forth-Systeme JTAG Booster. The 3rd connector with 20 pins is the Multi-ICE interface.

14-pin connector, X4		
Pin	**Signal**	**Function**
1	+3.3V	Power Supply for Adapter
3	NC	Not connected
5	TDI	Serial data input, to NET+ARM
7	TMS	Serial mode select
9	TCK	Serial clock
11	TDO	Serial data output, from NET+ARM
13	+3.3V	Power Supply for Adapter
2	GND	GND
4	GND	GND
6	GND	GND
8	GND	GND
10	GND	GND
12	TRST#	JTAG reset 1.)
14	GND	GND

1.) Per default the signal TRST# is not connected to the module, because there is a connection between TRST# and the system reset already on the module.

8 pin connector, X5		
Pin	**Signal**	**Function**
1	TCK	Serial clock
2	GND	GND
3	TMS	Serial mode select
4	TRST#	JTAG reset
5	NC	Not connected
6	TDI	Serial data input, to NET+ARM
7	TDO	Serial data output, from NET+ARM
8	+3.3V	Power supply for JTAG Booster

20 pin connector, X6		
Pin	**Signal**	**Function**
1	+3.3V	Reference power with current limitation
3	TRST#	JTAG reset
5	TDI	Serial data input, to NET+ARM
7	TMS	Serial mode select
9	TCK	Serial clock
11	RTCK	Serial clock return path
13	TDO	Serial data output, from NET+ARM
15	POWERGOOD	System reset
17	NC	Not connected
19	NC	Not connected
2	+3.3V	Power supply for adapter
4	GND	GND
6	GND	GND
8	GND	GND
10	GND	GND
12	GND	GND
14	GND	GND
16	GND	GND
18	GND	GND
20	GND	GND

4.2. Serial Interfaces

The Evaluation Board provides different kinds of serial interfaces. These are RS232, CAN, Ethernet and USB.

4.2.1. RS232

The Evaluation Board provides two RS232-interfaces; COM A and COM B. Both interfaces are fitted with 9-pin SUBD male connectors.

COM A is fully equipped with all handshake signals. So a modem connection can be easy supported.

COM B only provides the data lines TXD and RXD, without any handshake signals.

COM A, 9-pin connector, X7		
Pin	**Signal**	**Function**
1	DCD#	Data Carrier Detect
2	RXD	Receive data
3	TXD	Transmit data
4	DTR#	Data Terminal ready
5	GND	GND
6	DSR#	Data Set ready
7	RTS#	Request to send
8	CTS#	Clear to send
9	RI#	Ring indicator 1.)

1.) RI# is connected to the RS232 driver, but the signal cannot be monitored by any CPU pin.

COM B, 9-pin connector, X8		
Pin	**Signal**	**Function**
1	NC	Not connected
2	RXD	Receive data
3	TXD	Transmit data
4	NC	Not connected
5	GND	GND
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	NC	Not connected

4.2.2. CAN

The Evaluation Board provides two CAN interfaces; CAN1 and CAN2. CAN1 is fitted with a 9-pin SUBD male connector X9, while CAN2 is available at a 10-pin header with twin rows, X10.

Both channels provide the termination resistor, which can be disabled by removing jumper JP4 for CAN1 or JP5 for CAN2. There is also the possibility to place the CAN drivers on the Evaluation Board (this is the factory default), in case a module without CAN drivers is used. In this case the resistors R65, R70 for CAN1 and R81, R82 for CAN2, are not equipped and the resistors R71 for CAN1 and R83 for CAN2 are assembled on the Evaluation Board.

It is also possible to insert an opto-coupler for a galvanic isolation of the CAN channels. This can be done by removing R72, R73 for CAN1 or R84, R85 for CAN2 and connecting the wire from the opto-coupler to the pads of these resistors.

CAN 1, 9-pin connector, X9		
Pin	**Signal**	**Function**
1	NC	Not connected
2	CAN_L1	CAN low
3	GND	GND
4	NC	Not connected
5	NC	Not connected
6	GND	GND
7	CAN_H1	CAN high
8	NC	Not connected
9	NC	Not connected

CAN 2, 10 pin connector, X10		
Pin	**Signal**	**Function**
1	NC	Not connected
3	CAN_L2	CAN low
5	GND	GND
7	NC	Not connected
9	NC	Not connected
2	GND	GND
4	CAN_H2	CAN high
6	NC	Not connected
8	NC	Not connected
10	NC	Not connected

4.2.3. Ethernet

The Ethernet connection is realized by a standard 8-pin RJ45 module jack, X11. For additional information about the data flow, there are two LEDs.

LED LE2 shows the Link/Activity and LED LE3 is active for a 100Mbit connection.

4.2.4. USB

The Evaluation Board is prepared for future versions of the module which support a USB port. The Evaluation Board provides the possibility either to use the USB channel as a host or as a device. This functionality is chosen by the jumpers J13 and J14.

Configuration Jumper J13, J14

Configuration Jumper J13, J14		
Connected Pins	**Function**	**Used connector**
1-2	NET+ARM is USB host	USB type A, X12
2-3	NET+ARM is USB device	USB type B, X13

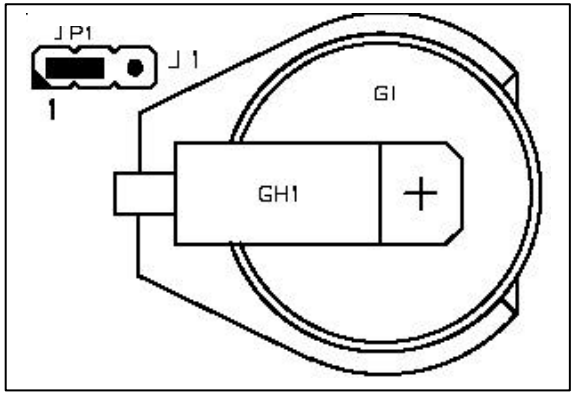
4.3. Power Supply

The Evaluation Board expects a stabilized 5 VDC (±0.25V) voltage at the X1 power connector.

4.4. Battery Back-up

A Lithium battery (3V) is also included on the Evaluation Board when shipped. It supplies both, low-powered SRAMs and the RTC on the module. According to the position of jumper J1 the battery can be connected or disconnected.

Configuration Jumper J1	
Connected Pins	**Function**
1-2	Battery connected
2-3	Battery disconnected



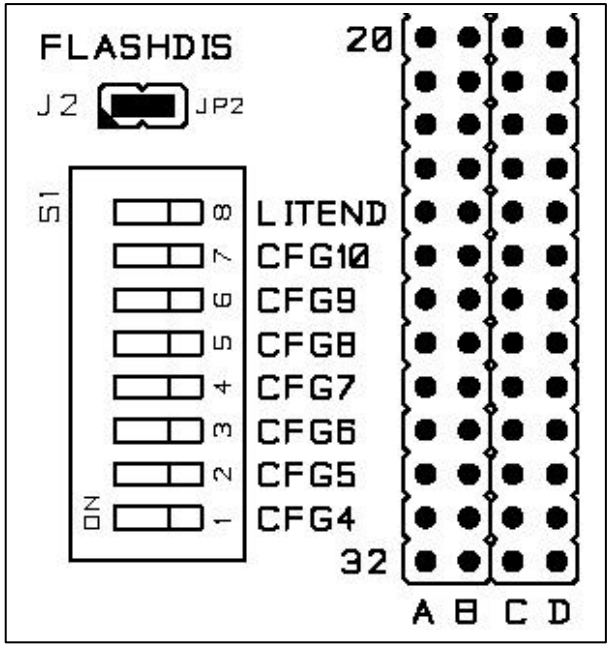
4.5. System Configuration

With the DIP switch S1 some configurations for the NET+ARM CPU can be made. The ON position generates a low-level at the CPU pin.

Configuration DIP switch S1	
Switch	**Function when ON**
1	CFG4 written to system status register bit4
2	CFG5 written to system status register bit5
3	CFG6 written to system status register bit6
4	CFG7 written to system status register bit7
5	CFG8 written to system status register bit8
6	CFG9 written to system status register bit9
7	CFG10 written to system status register bit10
8	Little Endian

With the jumper J2 the Flash memory on the module can be disabled. This is needed to enter the debugger, if the Flash memory is empty, for example. If the jumper J2 is open, the Flash memory is enabled.

Configuration Jumper J2	
Connected Pins	**Function**
1-2	Flash memory disabled



4.6. User Area

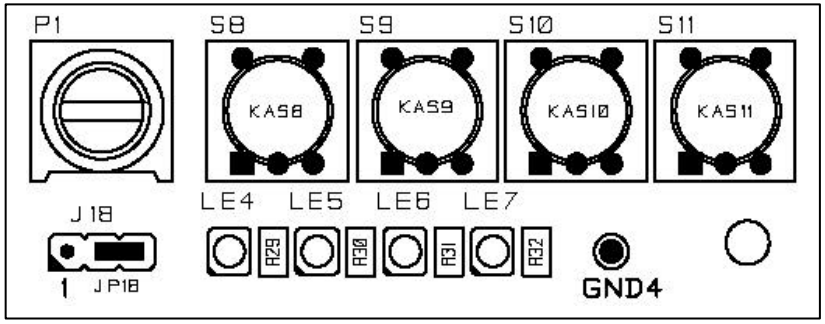
The Evaluation Board provides two expansion headers, 2x32 pins each (X16 and X17), with system and peripheral signals, a wire-wrap field, four LEDs, four push buttons, one potentiometer, one buzzer and a pulse generator; all of which can be freely used by the user.

Expansion connector X17(AB), X16(CD)				
Pin	**Row A**	**Row B**	**Row C**	**Row D**
1	Address A0	Address A1	Port A0	Port A1
2	Address A2	Address A3	Port A2	Port A3
3	Address A4	Address A5	Port A4	Port A5
4	Address A6	Address A7	Port A6	Port A7
5	Address A8	Address A9	Port B0	Port B1
6	Address A10	Address A11	Port B2	Port B3
7	Address A12	Address A13	Port B4	Port B5
8	Address A14	Address A15	Port B6	Port B7
9	Address A16	Address A17	Port C0	Port C1
10	Address A18	Address A19	Port C2	Port C3
11	RSTIN#	PWRGOOD	Port C4	Port C5
12	WE#	OE#	Port C6	Port C7
13	R/W#	TS#	PACK#	PEN#
14	BCLK	TA#	PINT1#	PINT2#
15	CS3#	TEA#	PDATA0	PA0
16	CS4#	BG#	PDATA1	PA1
17	BE2#	BR#	PDATA2	PA2
18	BE3#	BUSY#	PDATA3	PA3
19	CS2#		PDATA4	PA4
20	Data D16	Data D17	PDATA5	PA5
21	Data D18	Data D19	PDATA6	PA6
22	Data D20	Data D21	PDATA7	PA7
23	Data D22	Data D23	PDATA8	PA8
24	Data D24	Data D25	PDATA9	PA9
25	Data D26	Data D27	PDATA10	PA10
26	Data D28	Data D29	PDATA11	PA11
27	Data D30	Data D31	PDATA12	PA12
28			PDATA13	PA13
29			PDATA14	PA14
30	+ 3,3V	+ 3,3V	PDATA15	PA15
31	GND	GND	PCS#	PA16
32	+ 5V	+ 5V	PRW#	PBRW#

Generating Chip Select signals for the push buttons and LEDs		
Signal	CETAST# active	CELED# active
A11	1	0
A12	1	1
CS3#	0	0
OE#	0	X

With the jumper J18 either the output signal of the pulse generator U3 or the interrupt request signal of the CompactFlash card can be connected to the interrupt input port PORTC3 of the NET+ARM. If both signals are needed, one of them can be connected to a free port at the header X16 (CD) with a cable. With the potentiometer P1, the frequency of the square wave output signal of the pulse generator output can be varied between 1300Hz and 14kHz.

Configuration Jumper J18	
Connected Pins	**Function**
1-2	Interrupt Request from CompactFlash
2-3	Output signal of pulse generator



The four push buttons are not connected directly to port pins of the NET+ARM, but can be accessed by reading an 8-bit value from the address selected with CETAST#.

The 8-bit value has the following meaning:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	CD2#	CD1#	S11	S10	S9	S8

CD1# and CD2# are the card detect signals of the CompactFlash card.

The four LEDs are not connected directly to port pins of the NET+ARM, but can be accessed by writing an 8-bit value to the address selected with CELED#.

The 8-bit value has the following meaning:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NC	NC	NC	NC	LE7	LE6	LE5	LE4

Like the debug LED, the buzzer H1 is also connected to PORTA4. The buzzer can be disconnected by removing the jumper JP6.

Configuration Jumper J6	
Connected Pins	**Function**
1-2	Buzzer connected

4.7. CompactFlash

The Evaluation Board is equipped with a CFA Type 2 connector, X14, which is on the underside of the board.

The card can only be accessed as a Master in True IDE mode.

Generating Chip Select signals CEIDE1# and CEIDE2#		
Signal	**CEIDE1# active**	**CEIDE2# active**
A11	0	1
A12	0	0
CS3#	0	0
OE#	X	X

The card detect signals CD1# and CD2# can be read with the CETAST# chip select at Bit5 and Bit4 (see chapter 4.6).

When both bits are set to zero, the card is inserted.

4.7.5. CompactFlash, 50-pin connector X14

Pin	Signal name True IDE mode	Description
1	GND	GND
2	D3	Data D19
3	D4	Data D20
4	D5	Data D21
5	D6	Data D22
6	D7	Data D23
7	CEIDE1#	Card select signal 1 access to task file registers
8	A10	not used at True IDE mode
9	ATASEL#	low to select True IDE mode
10	A9	not used at True IDE mode
11	A8	not used at True IDE mode
12	A7	not used at True IDE mode
13	VCC	+ 3.3V
14	A6	not used at True IDE mode
15	A5	not used at True IDE mode
16	A4	not used at True IDE mode
17	A3	not used at True IDE mode
18	A2	Address A3
19	A1	Address A2
20	A0	Address A1
21	D0	Data D16
22	D1	Data D17
23	D2	Data D18
24	IOIS16#	not connected
25	CD2#	Card detect 2: high, if no card available
26	CD1#	Card detect 1: high, if no card available
27	D11	Data D27
28	D12	Data D28
29	D13	Data D29
30	D14	Data D30
31	D15	Data D31
32	CEIDE2#	Card select signal 2 access to alternate status register and device control register
33	VS1#	connected to +3.3V
34	IORD#	to read data in I/O task file area
35	IOWR#	to write data in I/O task file area
36	WE#	not used at True IDE mode

Pin	Signal name True IDE mode	Description
37	INTRQ	Interrupt request to the host (active high)
38	VCC	+ 3.3V
39	CSEL#	low to select Master
40	VS2#	connected to +3.3V
41	RESET#	active low Reset signal
42	IORDY	connected to +3.3V
43	INPACK#	not connected
44	REG#	connected to +3.3V
45	DASP#	not connected
46	PDIAG#	not connected
47	D8	Data D24
48	D9	Data D25
49	D10	Data D26
50	GND	GND

5. Changes to Revision EVANET_0

The following changes have been made:

- removed the jumpers for the CompactFlash, the CompactFlash is now only accessible as Master at True IDE mode.
- included a buzzer, connected to PORTA4 via jumper J6
- some wires have been taken over into the layout