Module
C167CR_2

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Stand 26.08.1998

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1. Introduction

The series of the pluggable, credit card sized CPU-Modules has a further member - the Module C167CR_2 with the Siemens CPU C167CR with an on chip CAN-Module. It combines high 16-Bit CPU performance with high peripheral functionality and enhanced I/O-capabilities. So, this module is the best choice for network real time applications.

The series of the modules are available with following MCU´s at time:

Module 6303	with Hitachi HD6303
Module 64180	with Hitachi HD64180
Module V25	with NEC V25
Module RTX2001	with Harris RTX2000/RTX2001
Module 68332	with Motorola MC 68332
Module 80C166	with Siemens SAB 80C166
Module C167CR	with Siemens C167CR
Module 80386EX-CAN	with Intel i386EX
Module 80386-DRAM	with Intel i386EX
Module ELAN386	with AMD ÉlanSC300
Module ELAN486	with AMD ÉlanSC400

The Module C167CR_2 is the successor of the Module C167CR. There are following differences between both modules:

- There are now 512 kByte Flash-EPROM onboard (optional 1 MByte) and furthermore, there are two PLCC-sockets for up to 1 Mbyte (Flash-) EPROM on the Module C167CR_2. So, it’s possible to run the module with 2 MByte (Flash-)EPROM.
- For special use of the Module C167CR_2, it can be equipped with with a F167-processor with 128 kByte internal Flash-EPROM. In this case, there are also 3 additional address lines available at the modules connector, but you have to work without the UART 16C550

Certainly, the Module C167CR_2 is pin-compatible to the Module C167CR. Applications built with the Module C167CR run also with the Module C167CR_2 - no changes at your hardware are necessary.

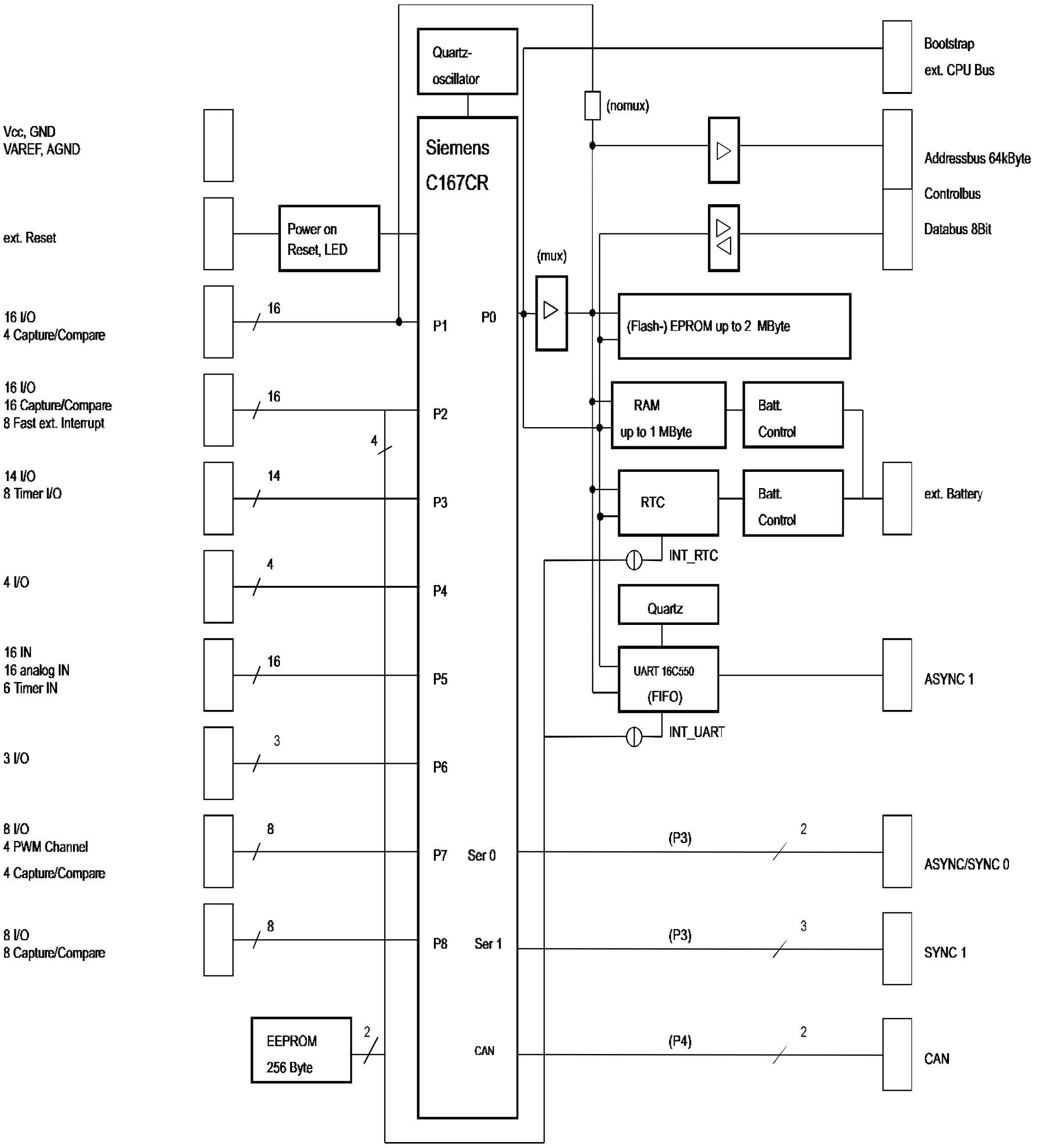
The Module C167CR_2 is available with multiplexed and non multiplexed bus. There are two fundamental differences between the two modules. One is the amount of the I/O ports - because of the multiplexed bus, this module has 16 I/O ports more than the non multiplexed module. The second difference is, that the non multiplexed module has a 50% higher computing speed at zero wait states because of the separated address and data busses. Both variants are hard wired, so you should exactly know which of both modules you want to order.

2. Features of the Module C167CR_2

- Compatible to the Module C167CR
- Processor Siemens C167CR, 16-Bit Controller with on chip CAN-Controller
- Quartz oscillator for 20 MHz CPU clock
- 100 ns instruction cycle time
- Resetcontroller, connectable with a push-button Reset
- Programmable Watchdog Timer
- 16 MByte linear address space for program and data
- 256 KByte static RAM, 0 wait states (optional 1 MByte)
- 2 KByte fast static RAM in the CPU
- up to 2 MByte Flash-EPROM
- 2 bytewide sockets (PLCC) for up to 1 MByte ROM or Flash-EPROM
- 512 kByte Flash-EPROM onboard (optional 1 MByte), 16 Bit, 1 wait state
- Flash memory in circuit programmable
- Flash-EPROM is supported via Bootstrap Loader
- Up to 2 kByte serial EEPROM on the module (256 Byte standard)
- Real-Time clock RTC72423, able to generate interrupts
- Battery backup unit for RTC and RAM
- LED function control
- All processor signals available on dual row pin header
  (except A16..A19 and D8..D15)
- External 8 Bit peripherals connectable
- 5 programmable chip-selects
- 2 serial channels (sync./async. and high speed synchronous), TTL-Level
- UART 16C550 with integrated FIFO for a additional serial interface with up to 115 kBaud, TTL-Level
- 16 channel 10-Bit A/D converter, 9.75µs conversion time
- 8 channel Peripheral Event Controller (PEC)
- 56 separate interrupt sources that may be assigned to 16 priority levels, 8 of them with fast external interrupt inputs (50ns sample rate)
- General purpose timer/counter with a resolution of 200/400 ns
- two 16-channel capture/compare module
- 4-channel PWM-module (up to 78 kHz)
- 83 I/O lines in the multiplexed version
- 67 I/O lines in the non multiplexed version
- Data-, address- and control bus buffered
- Power consumption about 5V / 200mA
- Mechanical dimensions 2.5" x 3.2" (63,5 mm x 81,28 mm)

- The module is pluggable with two robust 2 x 32 -pin Berg connectors

3. Block Diagram



4. Getting started..

4.1 ..with the Evaluation Board EVA167

With the help of this evaluation board you can easily put the Module C167CR_2 into operation without further external connections. All features of the module are supported.

The serial interface ASC0 of the target must be connected to a standard serial port of a PC (COM1 or COM2). The COM ports must be able to generate hardware interrupts, IRQ4 for COM1 or IRQ3 for COM2.

Now you can test your module by loading a program to RAM or program it to EPROMs or Flash-EPROMs.

See chapter "8. Evaluation Board EVA167" for more informations about the evaluation board.

4.2 ..without the Evaluation Board EVA167

If you do not use the Evaluation Board EVA167, you have to connect your Module C167CR_2 as follows:

Signal	**Pin of 128 pol connector**	**Comment**
GND	32, 64	ground connection
+5V	65, 97	supply voltage +5V ±0.25V, typical 200mA current consumption
BATT	98	either a 3V battery voltage or a connection to ground
VAREF	31	reference voltage for A/D converter, i.e. connected with +5V

To connect the Module C167CR_2 with a PC via a V24/RS-232 interface, you need an external driver device (for example MAX233) to adapt the TTL signals to the RS232 voltage levels.

See chapter "7. Bootstrap function" for more information about the Bootstrap Loader Mode.

4.3 EPROMs

There are now 512 kByte Flash-EPROM onboard (optional 1 MByte) and furthermore, there are two PLCC-sockets for up to 1 Mbyte (Flash-) EPROM on the Module C167CR_2. So, it’s possible to run the module with 2 MByte (Flash-) EPROM. (See chapter "11. Special Configurations".)

For the use of further (Flash-) EPROMs, the PLCC-sockets can be equipped with CMOS-EPROMs of the sizes 128k*8-Bit (27C010) or 256k*8-Bit (27C020) as well as Flash-EPROMs of the sizes 128k*8-Bit (Am29F010) or 512k*8-Bit (Am29F040). That makes a modification of solder bridge LB5 necessary: it must be opened to disable chip select -CS0 for the Onboard-Flash. The table below gives you an overview:

EPROM (Manufactors Code)	**Type**	**Size**	**LB5**	**Comment**
Am 29F400 onboard (standard)	Flash-EPROM	256k*16	closed	
2 x 27C010 on PLCC	EPROM	2 x 128k*8	opened	onboard Flash disabled
2 x 27C020 on PLCC	EPROM	2 x 256k*8	opened	onboard Flash disabled
2 x Am29F010 on PLCC	Flash-EPROM	2 x 128k*8	opened	onboard Flash disabled
2 x Am29F040 on PLCC	Flash-EPROM	2 x 512k*8	opened	onboard Flash disabled

It's recommended to use only AMD Flash-EPROMs for best compatibility:

- Am29F010 (128k*8)
- Am29F040 (512k*8)

Connect the EPROMs with the module in such way, that the lower (even) bytes are connected with the inner socket (U5) and the higher (odd) bytes are connected with the socket at the edge (U4).

A reset pulse with defined length will be generated automatically, after initial assertion of the power supply. So, the CPU will be reset and begins with the processing of the first instruction at address 0. Note that the EPROM area is selected via chip-select -CS0 at this address. The programmable chip-select signals are generated by the CPU (see chapter "6. Memory Mapping").

4.4 Using a ROM-Emulator

Two PLCC sockets are equipped on the module to plug in Flash-EPROMs or to connect a ROM-Emulator. In this case, the onboard Flash-EPROM must be switched off by oppening the solder bridge LB5.

4.5 Running the first program

In this chapter, you can see how to program the small example EPROM.BIN into the Flash-EPROM on your Module C167CR_2.

This example shows the usage of the RTC 72423 on the FS FORTH-SYSTEME Module C167CR_2. After reset, the RTC is checked for valid values. If the read values are incorrect, the RTC is reset to a default time. The time is printed every second at ASC0 (TXD0) and the LEDs on port P2.0 to P2.7 are shifted down.

Act as follows, to get EPROM.BIN into the Flash-EPROM:

- bring your Module C167CR_2 into the Bootstrap Mode (close Jumper J2 on the evaluation board EVA167 - Signal P0L.4 of the CPU must be sampled low at the end of a hardware reset)
- connect your module with the serial interface of your PC
- copy ..\EXAMPLES\RTC167\EPROM.BIN from the FS FORTH-SYSTEME support disk to your hard disk
- install the FLASH166 software on your system; it's recommended to copy the FLASH166 files (FLASH166.EXE + FLASH166.OVL) to the binary path of your compiler
- be sure, the settings of the paths are correct, because your system must find the FLASH166 software
- type "FLASH166 /P EPROM.BIN" at the DOS prompt and press <Return> - type "FLASH166 /P EPROM.BIN /COM2" for the second serial interface of your PC
- remove the bootstrap jumper and press the reset button - the program starts

4.6 Software

We offer efficient software like:

- FLASH166 software for a easy programming of the Flash-EPROM
- Keil and Tasking (free demo) C-Compiler with restricted code size
- PLS debugger (free demo) fast-view66/WIN, which is a high level language debugger for windows. It allows a fast and reliable start and test of applications, which are programmed in C and/or assembler

The FLASH166 software is free of charge if you buy this module. This program uses the Bootstrap Mode of the Siemens 80C166 microcontroller family

- to program data into Flash memory
- to load data into static RAM
- to make a memory dump
- to test CPU pins

All functions are realized by a monitor program running in the internal memory of the microcontroller.

5. Module C167CR_2

5.1 Connection

The module has two 2 x 32 - pin Berg connectors with 128 connections total at the bottom. These 128 connections are containing all necessary signals for an application: voltage supply, buffered busses, ports, control lines, and so on.

5.2 Power supply

The +5V supply voltage is connected to pin 65 and 97 and has to be stabilized more exactly than ±0.25V. At normal 20 MHz CPU clock, the current consumption is about 200mA.

Battery voltage BATT at pin 98:
The battery voltage BATT from a lithium battery of about 3V is needed to retain data in the RAM and for an undisturbed operation of the real time clock at power failure. If you want to do without battery, you have to connect the input BATT with GND. Only a few µA current consumption are needed for the battery, and it will be reduced to about 100nA if the supply voltage of 5V is applied to the board.

GND at pin 32 and 64:
Ground of the supply voltage.

VAGND at pin 63:
The ground of the analog-digital-converter is on a node connected with GND of the module. This node can be opened for special use.

Reference voltage VAREF at pin 31:
The reference voltage (4.8V < VAREF < 5.2V) of the analog/digital converter has to be applied here. This connection has always to be connected, for example with +5V of the supply voltage. To utilize the full resolution of the A/D converter it's recommended to use a separate stabilized reference voltage.

5.3 Control signals

Reset-input -RESET at pin 66:
With the signal -RESET, the module can be reset to a defined state. A reset button can be connected directly to this input. A hardware reset is triggered with the help of signal -RSTIN (-RSTIN is connected with the reset controller MAX704) when the supply voltage is applied to the board. In any case the RAM is protected against random overwriting.

Reset-output -RSTOUT at pin 71:
The Siemens C167CR has the special instruction EINIT, which indicates the end of initialization at the output -RSTOUT. To get a good reset condition for the periphery at all reset-causes (hardware reset, software reset, watchdog), the pin -RSTOUT of the processor is available at the Berg connector. The state of -RSTOUT is shown via an LED on the module. As long as the LED is off, no EINIT-instruction has been executed since the last reset.

Bootstrap-enable -BOOTSTR at pin 81:
To activate the Bootstrap Mode, the input -BOOTSTR has to be connected with GND. After the next hardware reset (no software reset or reset via watchdog), the processor branches to the bootstrap function.

Non-maskable interrupt -NMI at pin 37:
The non-maskable interrupt input is connected to +5V through a resistor - so there is no further connection necessary.

Chip-select external -CSEXT at pin 103:
This signal is for the selection of the external periphery and free programmable. If there’s only one external device, the device can be selected directly via -CSEXT (see chapter "6. Memory mapping").

Write enable -WRL at pin 108 :
The write enable signal (Low Byte) is bufferd available at the Berg connector
See also Port 3, P3.12/-BHE/-WRH.

Read enable -RD at pin 105:
The read enable signal is buffered available at the Berg connector.

Clock output at pin 117:
At port P3.15 the system clock can be fetched out. To get the system clock at port P3.15, this must be enabled via software. Otherwise this port is used as normal I/O port.

5.4 Address Bus

Address Bus A0-A15:
Here are the address lines of the external 64kByte addressbus buffered available for read and write access. They are independent of the multiplexed or the non multiplexed version. At the non multiplexed version, these signals have to be used (not the unbuffered port 1), too.

Address-Latch-Enable ALE at pin 76:
This buffered output indicates the beginning of a bus cycle.

5.5 Port 1

P1L.0 to P1L.7:
In multiplexed version of the module, this port is available as a 8-Bit bidirectional I/O port.

P1H.0 to P1.H7:
In multiplexed version of the module, this port is available as a 8-Bit bidirectional I/O port.

Please Note: The connections P1H.4/CC24IO to P1H.7/CC27IO are additionally connceted with the capture compare unit.

5.6 Port 2

P2.0/CC0IO to P2.7/CC7IO:
This is a bidirectional I/O port, which is additionally connected with the capture compare unit.

P2.8/CC8IO/EX0IN
This is a bidirectional I/O port, which is also connected with the capture compare unit. Moreover, here is a fast external interrupt input with 50ns sample rate available. The interrupt output of the real time clock 72423 is connected to this signal, if the solder bridge LB1 is closed.

P2.9/CC9IO/EX1IN
This is a bidirectional I/O port, which is also connected with the capture compare unit. Moreover, here is a fast external interrupt input with 50ns sample rate available. The interrupt output of the UART 16C550 is connected to this signal, if the solder bridge LB2 is closed.

P2.10/CC10IO/EX2IN to P2.15/CC15IO/EX7IN/T7IN
This is a bidirectional I/O port, which is also connected with the capture compare unit. Moreover, here are further fast external interrupt inputs with 50ns sample rate available. Connection P2.15/CC15IO/EX7IN/T7IN is additional connected with the timer T7 count input.

Therefore, port 2 can not only be used as a normal input/output (every pin separate), but also as an interrupt input and for pulse measurement or generating.

5.7 Port 3

Because all connections of port 3 have multiple functions, all ports will be descriped individually. If you don't want to use the special function, you can use the corresponding pin as a bidirectional I/O port. That concerns to P3.0 to P3.11 as well as P3.13 and P3.15. Every connection is used as port and as a special function and both signals combined (logical ANDed). To use for example P3.10 as an asynchronous interface output (TXD0), P3.10 has to be an output with a high level. Therefore, you can always test the level of an input port with special function via software.

P3.0/T0IN a pin 91:
Input to CAPCOM timer T0 in counter mode. The timer 0 is one of the both timers, which are used as reference to the Capture Compare block. It can work synchronous to the system clock as well as fed with an external signal, which has to be applied at this connection. The frequency must be smaller than 1.25 MHz.

P3.1/T6OUT at pin 123:
The GPT2 timer T6 is a system clock-synchronous up/down counter via software, of which overflows can change the level at T6OUT (level changes at every under- or overflow). So, every frequency from 0.07 Hz up to 2.5 MHz can be generated. For example, a simple digital PLL circuit is possible in combination with P3.2/CAPIN.

P3.2/CAPIN at pin 92:
This pin also belongs to the GPT2 block (Timer T5 and T6). Depending on the selected edge (register T5CON), the register CAPREL can be loaded with the content of T5 via a signal at this connection. An interrupt condition will be generated. Therefore, this pin can be used only as interrupt input. Moreover, at loading, T5 can be erased at the same time.

P3.3/T3OUT at pin 124:
This function is nearly similar to T6OUT. To signal the zero crossings of T3, P3.3 has to be set to an output(via DP3) and T3OE(T3CON.9) to high level. Therefore, T3OUT follows T3OTL(T3CON.10).

P3.4/T3EUD at pin 93:
If T3UDE = 1(T3CON.8), T3 counts up in case of the level at T3EUD is of the same content as T3UD(T3CON.7). Otherwise, T3 counts down.

P3.5/T4IN at pin125:
In counter-mode (T4M = 1 and T4I = 2, 3 or 4, both at T4CON), the pulses at T4IN will be counted (frequency smaller than 1.25 MHz). The from the system clock resulting pulses (fosc*2^(-16-T4I)) will be counted in the gated timer mode, if the correct level (T4M = 2 or 3 at T4CON) appears at this pin. In reload mode (T4M = 4), T3 will be loaded with the current content of T4, if a correct edge changing occurs at T4IN (T4IN = 0 to 3). In capture-mode (T4M = 5), T4 is loaded with the content of T3.

P3.6/T3IN at pin 89:
In counter-mode (T3M = 1 and T3I = 1 to 3, both at T3CON), the matching edges at T3IN will be counted from T3. Information about the counter advance sense can be deduced from P3.4/T3EUD. The frequency has also to be smaller than 1.25 MHz. The same as P3.5/T4IN is for the gated-timer-mode
(TM3 = 2, 3).

P3.7/T2IN at pin 120:
See P3.5/T4IN.

P3.8/MRST at pin 88:
Master receive / slave transmit of the serial interface, channel 1.

P3.9/MTSR at pin 119:
Master transmit / slave receive of the serial interface, channel 1.

P3.10/TxD0 at pin 87:
Output of the serial interface, channel 0. In asynchronous mode, this is the output of the serial data transmission. Attention: This connection has CMOS level. For the most data transmissions, external drivers are necessary (for example a MAX 233 for a V24/RS232 interface). In synchronous mode, this pin is the clock signal.

P3.11/RxD0 at pin 118:
Input of the serial interface channel 0. In synchronous mode, this is the data input as well as the data output. For informations about levels and formats, see P3.10/TxD0.

P3.12/-BHE/-WRH:
Because this signal is internal used, it has to be set to an output with high level and to be activated in the SYSCON register with one of the first instructions. It's only available at the pin strip J1 and not at the Berg connector. See write enable -WRL (in chapter "5.3 Control signals") .

P3.13/SCLK at pin 86:
Master clock output / slave clock input of the synchronous serial interface, channel 1.

P3.14:
Through lack of pins at the package of the Siemens C167CR, this port is not available.

P3.15/CLKOUT at pin 117:
See clock output CLKOUT.

5.8 Port 4

P4.0/A16 to P4.3/A19:
This are the internal used, higher addresses A16 to A19.

P4.4/A20 at pin 84:
This pin can be used as a bidirectional I/O port, because address A20 is not used.

P4.5/A21/CAN_RXD(CANL) at pin 115:
For the Siemens C167CR, the port P4.5 is the RxD signal of the integrated CAN-controller. As an option, the module can be equipped with a CAN driver 82C250. In this case, the pin 115 feeds the signal CANL instead of the signal CAN_RxD.

P4.6/A22/CAN_TXD(CANH) at pin 83:
For the Siemens C167CR, the port P4.6 is the TxD signal of the integrated CAN-controller. As an option, the module can be equipped with a CAN driver 82C250. In this case, the pin 83 feeds the signal CANH instead of the signal CAN_TxD.

P4.7/A23 at pin 114:
This pin can be used as a bidirectional I/O port, because address A23 is not used.

5.9 Port 5

Port 5 is either a CMOS input-port with Schmitt trigger function or the input to a 16-channel multiplexer for the analog/digital-converter. The digital levels of these inputs can be read at register P5. The multiplexer is programmed via the Bits ADCH (in ADCON). Via ADDAT, you get the channel number in the upper 4 Bits which matches with the result. The availability of a result is signaled through ADCIC and errors through ADEIC. See also VAGND and VAREF (chapter 5.2 Power Supply) fore more information.

5.10 Port 6

P6.0/-CS0 to P6.3/-CS3:
This are the internal used , free programmable chip-select outputs (see chapter "6. Memory mapping").

P6.4/-CSEXT at pin 103:
See chip-select external (in chapter "5.3 Control signals").

P6.5/-HOLD at pin 13:
Because the signal -HOLD is not used, this connection can be used as a bidirectional I/O port.

P6.6/-HLDA at pin 46:
Also the signal -HLDA is not used - so this connection can be used as a bidirectional I/O port.

P6.7/-BREQ at pin 14:
Because the signal -BREQ is not used, this connection can be used as a bidirectional I/O port.

5.11 Port 7

P7.0/POUT0 to P7.3/POUT3:
This is a bidirectional I/O port, which can additionally be used as a pulse-width output.

P7.4/CC28IO to P7.7/CC31IO:
This is a bidirectional I/O port, which is additionally connected with the capture compare unit.

5.12 Port 8

P8.0/CC16IO to P8.7/CC23IO:
This is a bidirectional I/O port, which is additionally connected with the capture compare unit.

6. Memory Mapping

The memory mapping is determined via the free programmable chip select outputs of the Siemens C167CR. The chip select signals on the module are reserved as follows; **the address ranges are only suggestions:**

Address range	Chip select	Bus width	Function
40 FFFF 40 0000	-CS4	8 Bit	-CSEXT for 64 kByte external periphery
20 1FFF 20 1000	-CS3	8 Bit	UART, 4 kByte
20 0FFF 20 0000	-CS2	8 Bit	RTC, 4 kByte
1F FFFF 10 0000	-CS1	16 Bit	RAM up to 1Mbyte
0F FFFF 00 0000	-CS0	16 Bit	(Flash-) EPROM up to 1 MByte

After a reset, the CPU fetches the first instruction from address 0. Because only the chip select signal -CS0 is active after a reset, the Flash-EPROM will be detected at this address. If there is a program in the EPROM, it will automatically be started after a reset.

To use the PEC, you have to use the internal RAM or the XRAM, because the EPROM is mapped into the first segment of the memory.

7. Bootstrap Function

The Siemens C167CR has a built-in Bootstrap Loader, which provides a mechanism to load the startup program, which is executed after reset, via the serial interface. The Bootstrap Loader moves code/data into the internal RAM. Therefore it's possible to load a small program into the internal RAM and start it afterwards. It may be used to load the complete application software into ROMless systems, to load temporary software into complete systems for testing or calibration, or it may also be used to program Flash devices.

The Siemens C167CR enters Bootstrap Loader Mode, if pin P0L.4 is sampled low at the end of a hardware reset. In this case, the built-in Bootstrap Loader is activated independent of the selected bus mode. The Bootstrap Loader code is stored in a special Boot-ROM, no part of the standard mask ROM or Flash memory area is required for this.

(See "C167 User's Manual")

8. Evaluation Board EVA167

8.1 Features of the Evaluation Board EVA167

Features :

- Power supply by delivered power plug 220VAC/5VDC
- interface cable for the COM port on your PC
- Reset switch
- Lithium battery for RAM, 3V
- Two mounted RS232 and one CAN-driver
- frontal DSUB9 connector for the first RS232 interface (without handshake)
- frontal DSUB9 connector to interface to the CAN-Bus with transfer rates up to 1MBit/s
- 10-pin connector for the second serial interface (with RTS-CTS handshake)
- Jumper for BOOTSTRAP enable
- pluggable LED-row on port P2.0 to P2.7, inclusive power-on display
- pluggable DIP-switch on port P8.0 to P8.7
- pads and fastening-holes for a DIN 41612 plug

All connections of the module are as pads available on the evaluation board, and on a solder and wrap field there is enough place for further electrical groups.

In case of power failure, a high quality lithium battery will save the data in the RAM.

8.2 Interfaces of the Evaluation Board EVA167

Connector X1:

- CAN-Interface
- D-SUB, 9 pole, male

Pin	**Signal**
1	NC
2	CAN_L
3	GND
4	NC
5	NC
6	GND
7	CAN_H
8	NC
9	VCC (+5V)

Connector X2:

- RS232 interface ASC0
- D-SUB, 9 pole, female
- no handshake

Pin	**Signal**
1	NC
2	TXD0
3	RXD0
4	NC
5	GND
6	DTR0
7	NC
8	NC
9	NC

Connector X3:

- RS232 interface 16C550
- Berg connector, 10 pole
- handshake with RTS and CTS

Pin	Signal
1	NC
2	DTR1
3	TXD1
4	CTS1
5	RXD1
6	RTS1
7	NC
8	NC
9	GND

Connector X4:

- Power 5V

Pin	Signal
1	+5V
2	GND

8.3 Jumper configuration of the Evaluation Board EVA167

Jumper configurations:

Jumper	Function
J1, position 1-2 (closed at the side near R31)	Enable the use of the battery
J1, position 2-3 (closed at the side near reset switch)	Disable the use of the battery
J2, closed	Bootstrap Loader Mode
J3, closed	Connect CAN_L with CAN_H via a 120Ω resistor, to get a line termination.

8.4 Further important connections and components

The 0Ω resistors R17 and R18 are necessary, to bring the signals CAN_TXD and CAN_RXD to the connector X1, if there is no CAN driver on the board.

If you want to use optocouplers to separate the CAN driver from the module, remove the 0Ω resistors R29 and R30 and supply the CAN driver with an external supply voltage. Remove the 0Ω resistors R19 and R20 to connect the inputs and the outputs with the corresponding signals of the optocoupler.

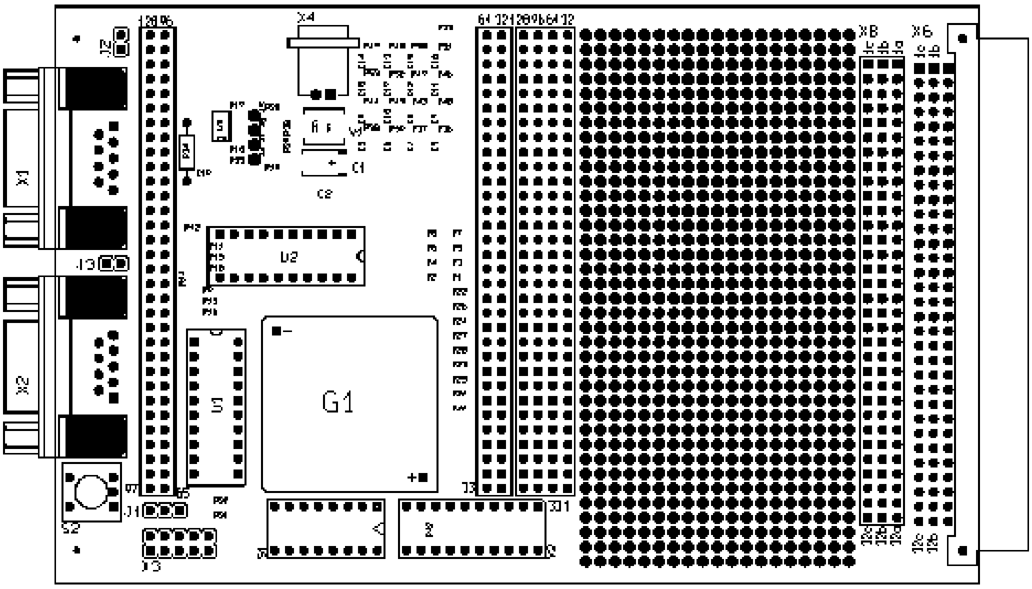
The pluggable LED-row is connected with port P2.0 to P2.7, -RSTOUT and the power supply :

LED..	is connected to..
LED1 .. LED8	P2.0 ..P2.7
LED9	-RSTOUT
LED10 (near dip switch)	Power supply

LED1 to LED8 are on, if the corresponding port pins P2.0 to P2.7 are LOW!
LED9 is on, if -RSTOUT = LOW (before the software instruction EINIT is executed). LED10 signals the supply voltage.

The pluggable DIP-switch S1 is connected with the corresponding ports P8.0 to P8.7.

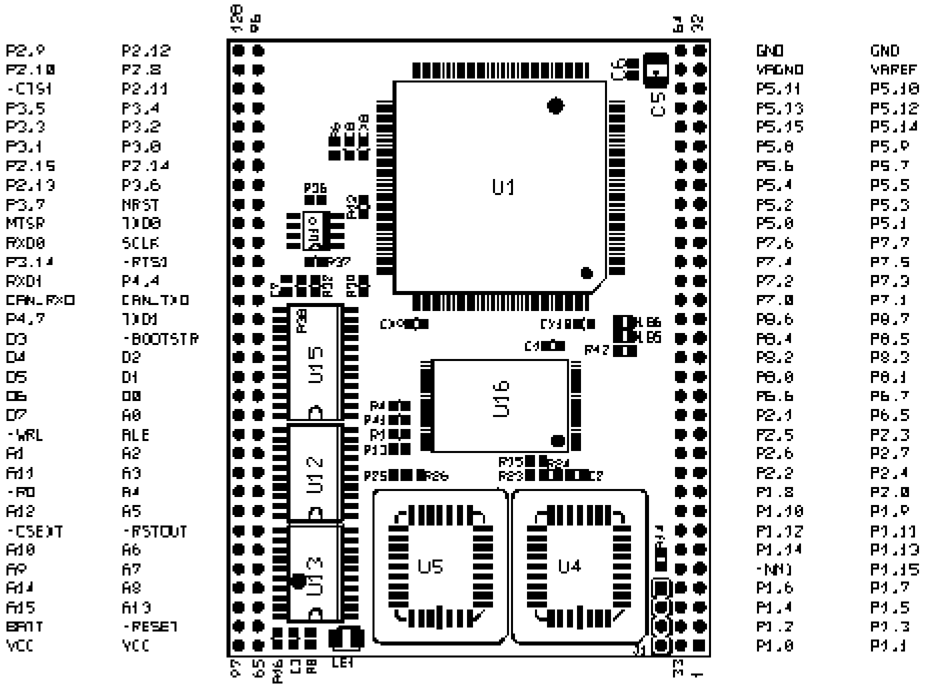
8.5 Layout of the Evaluation Board EVA167



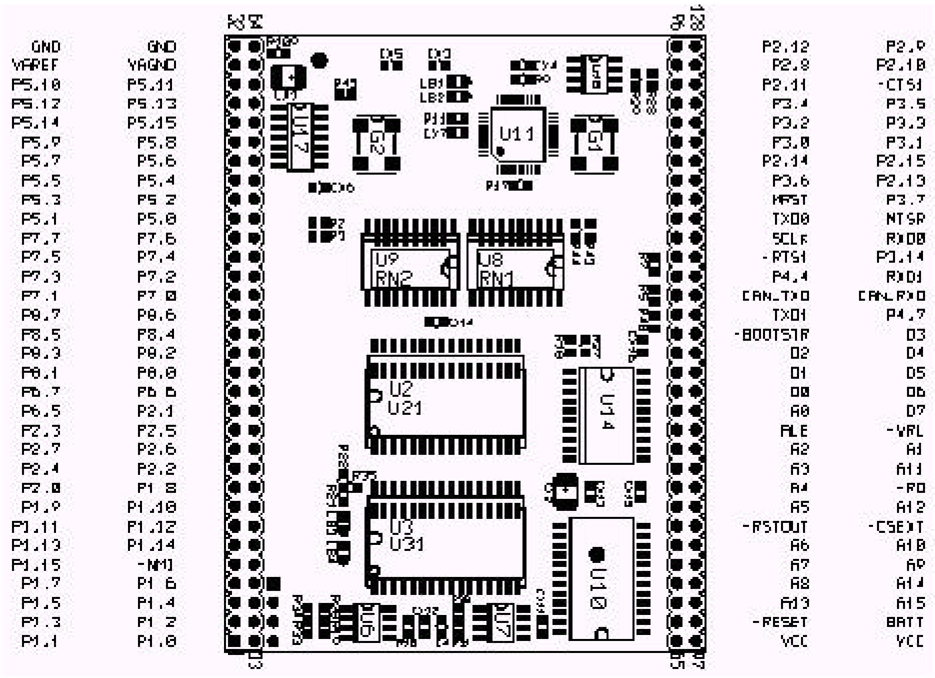
Size : 100mm x160mm

9. Layout of Module C167CR_2

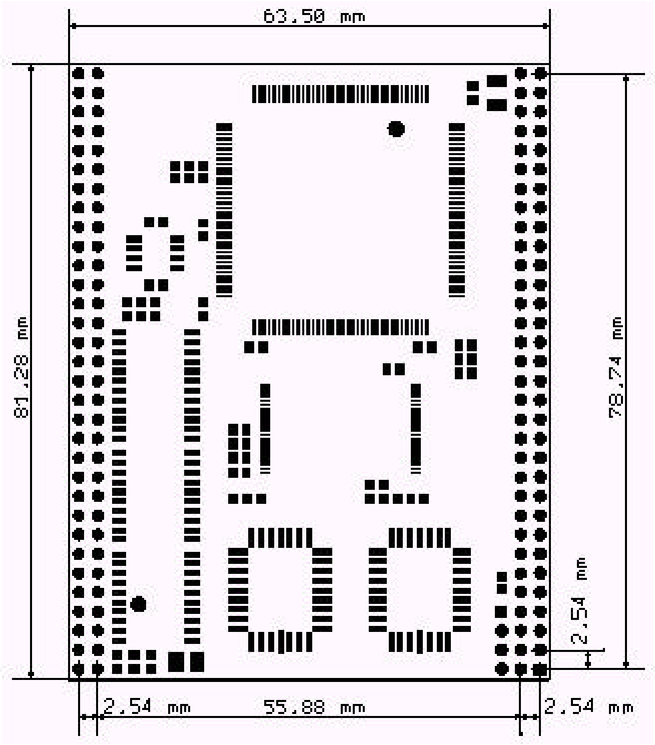
9.1 Top View



9.2 Bottom View



9.3 Dimensions



10. Software

10.1 Keil Compiler: Adapting the monitor (version V3.x)

It's necessary to adapt the monitor for the Module C167CR_2, because the hardware will not work with the standard files of the Keil monitor.

After you have installed the Keil development tools (full version or demonstration version), you have just to copy the files from the Keil..\MON166 directory of your FS FORTH-SYSTEME support disk to the corresponding directories on your hard disk. Be sure the settings of paths and environments are correct (see the file ..\C166EVAL.BAT for example)!

It's recommended to install the Keil software into the path \C166EVAL to avoid modification of the path names.

To adapt the monitor, see ..\MON166\README2.TXT .

If you want to use the bootstrap loader, use the following invocation:

```
"INSTALL  FOR7  0  100  102  BOOTSTRAP"
```

To verify the correct installation of the monitor, start the program MON166.EXE. If the system prompts:

```
        **** Monitor Mode ****
        #
```

everything is ok. Press F1-key to terminate the monitor program.

If you want to use monitor EPROMs, then you can use the existing binary file ..\MON166\MONFOR7.BIN from your FS FORTH-SYSTEME support disk. To program this file into Flash-EPROMs, just use the batchfile PROGFOR7.BAT. Verify the correct installation with MON166.EXE.

This adaptation is valid for the version V3.x of the Keil Compiler. It's possible, that the adaptation for higher versions are a little different. **So it's recommend to read the current text files of the FS FORTH SYSTEME support disk !**

10.2 Keil Compiler: Further adaptations (Version3.x)

It's recommended to copy all files from the FS FORTH-SYSTEME support disk to the corresponding directories. Especially the adapted startup file ..\LIB\STRTFOR7.A66 is needed to run the module.

The startup code is executed after processor reset and provides the startup sequence for the FS FORTH-SYSTEME Module C167CR_2. For example, the startup code assigns the chip selects to the EPROMs of the Module C167CR_2.

The startup object file should be linked to your application (click "Project|Compile File" in µVision-166 to generate the object file). An example is given by the ..\EXAMPLES\RTC167\RTC167.LIN file for µVision-166 (see chapter "10.3 Keil Compiler: Tools"):

```
rtc167.obj, \c166eval\lib\strtfor7.obj to rtc167.
```

This line in RTC167.LIN links and locates RTC167.OBJ and STRTFOR7.OBJ to the absolute file RTC167.

10.3 Keil Compiler: Tools (version V3.x)

The current tools (version V3.x) of the Keil Compiler are µVision-166 and dScope-166.

With µVision-166 you can edit and manage complete projects. This includes the assembler, compiler, linker and the object-hex converter.

To debug your application in a Windows environment, you can use the dScope-166 debugger or the high performance PLS debugger fast-view66/WIN.

10.4 Keil Compiler: Examples (version V3.x)

Certainly, examples can be found on the FS FORTH-SYSTEME disk (..\EXAMPLES).

Now, we step the RTC167 example (see the chapter "4.4 Running the first program" for description):

- open µVision/166 from the Windows desktop
- click "Project|OpenProject" and open \EXAMPLPES\RTC167.UVI\RTC167.PRJ
- click the "BuildAll" button
- click the "Debug" button, dScope-166 will be started and RTC167. will automatically be loaded into the RAM of your module
- type "g" for go, the program starts
- watch the Serial I/O window, time and date should be printed

See ..\EXAMPLES\RTC167\EPROM.BAT for an example, how to generate a project (compile, link,..) and program this into the Flash-EPROM. This example is ready to use with DOS or in a DOS-Box.

10.5 Tasking Compiler: Adapting the monitor (version V5.x)

It's also necessary to adapt the Tasking monitor for the Module C167CR_2, because the hardware will not work with the standard files.

After you have installed the Tasking development tools (full version or demonstration version) you have just to copy the files from the Task..\ETC directory to the corresponding directory on your hard disk. Be sure the settings of paths and environments are correct (see ..\SETPATH.BAT for example)!

The modified TARGET.CFG file contains information about the Module C167CR_2 for the XVW166 debugger. Now the FS FORTH-SYSTEME module can be selected in the "startup options|CPU type" of the debugger. Don't forget to choose the correct serial interface in the "Communication setup".

Attention: If you execute XVW166E.EXE, then the module is the target. For simulation, use XVW166S.EXE .

This adaptation is valid for the version V5.1R0 of the Tasking Compiler. It's possible, that the adaptations for later versions are a little different. **So it's recommended to read the current text files of the FS FORTH SYSTEME support disk!**

10.6 Tasking Compiler: Further adaptations (version V5.x)

It's recommended to copy all further files from the FS FORTH-SYSTEME support disk to the corresponding directories.

Especially the adapted startup file ..\LIB\STRTFOR7.ASM is needed to run a application from the onboard Flash-EPROM. For example, the startup code assigns the chip selects to the EPROM and RAMs of the Module C167CR_2.

The startup object file should be linked to your application. An example is given by the ..\EXAMPLES\BLINK.EPR\EPROM.BAT file on your support disk, which runs under DOS:

After the macro preprocessor has generated strtfor7.src from strtfor7.asm and the assembler made the object file, the linker is invoked:

```
l166 link strtfor7.obj, blink.obj ext\c166s.lib to blink.lno
```

The linker uses the library for the extended C167 instruction set.

10.7 Tasking Compiler: Tools (version V5.x)

The important current tools (version V5.1) of the TASKING Compiler are EDE and the XVW166 debugger.

With EDE you can edit and manage complete projects. This includes the assembler, compiler, linker and the hex converter.

To debug your application in a Windows environment, you can use the XVW166 debugger or the high performance PLS debugger fast-view66/WIN.

10.8 Tasking Compiler: Examples (version V5.x)

Certainly, examples can be found on the FS FORTH-SYSTEME support disk (..\EXAMPLES).

See ..\EXAMPLES\BLINK.DEB\.. and ..\EXAMPLES\BLINK.EPR\.. for examples, how to generate a project (..,assemble, compile, link, locate..) in a DOS environment.

The batch file ..\EXAMPLES\BLINK.DEB\MAKEABS.BAT generates the loadable absolute file BLINK.ABS for the cross view debugger XVW166.

The batch file ..\EXAMPLES\BLINK.EPR\EPROM.BAT generates the loadable binary file BLINK.BIN and programs it with the tool FLASH166.EXE into the Flash-EPROM.

See ..\EXAMPLES\BLINK.DEB\BLINK.C and
..\EXAMPLES\BLINK.EPR\BLINK.C for program description.

The program ..\EXAMPLES\BLINK.DEB\BLINK.C sets P2.0-P2.8 alternately to high and low.

..\EXAMPLES\BLINK.EPR\BLINK.C also sets P2.0-P2.8 alternately to high and low. Besides, it shows how to use the serial interface with the Tasking C-Compiler. To use output functions like printf or putch, the empty function _iowrite has to be filled, because the output functions use _iowrite.

It's recommend to look at the current files of the FS FORTH SYSTEME support disk for more examples and current informations !

11. Special Configurations

11.1 One MByte Flash-EPROM onboard

Optional, it's possible to run the module with an Am29F800 Flash-EPROM of the size 512k*16-Bit instead of the Am29F400 (standard) with 256k*16-Bit. This option should be ordered together with the Module C167CR_2.

11.2 One MByte (Flash-) EPROM on the PLCC-sockets

If you want to equip the module with 1 MByte (Flash-) EPROM, the standard configuration must be changed:

EPROM (U4/U5)	Size	LB3	LB4	LB5	LB6	R23	R24	R25	R26	R33	R34
Standard (Onboard-Fl. Enabled)	256k*16-Bit	X	-	X	-	X	-	X	-	X	X
2 * 29F040 on PLCC (Onboard-Fl. disabled)	2 * 512k*8	X	-	-	-	X	-	X	-	X	-
2 * 27C040 on PLCC (Onboard-Fl. disabled)	2 * 512k*8	X	-	-	-	-	X	-	X	-	X

X = solder bridge closed or resistor equipped
- = solder bridge is opended or resistor is removed

For the usage of 29F040 Flash-EPROMs without Onboard-Flash, you have just to disable CS0 for the Onboard-Flash via opening the solder bridge LB5. Additional, there are configurations on R23-R26 and R33-R34 necessary to equip the PLCC sockets with 27C040 EPROMs.

11.3 Two MByte Flash-EPROM on the Module C167CR_2

For the most applications, the standard 512kByte Flash-EPROM (AM29F400) onboard is enough. Nevertheless, the Module C167CR_2 can run with two MBytes Flash-EPROM. That means one MByte Flash-EPROM (Am29F800) onboard and one MByte Flash-EPROM (2 x Am29F040) on PLCC-sockets. This option should be ordered together with the Module C167CR_2.

Note, that the UART 16C550 has to be removed for this special use, because the chip select -CS3 of the UART is needed for the Onboard-Flash. Chip select -CS0 selects the Flash on PLCC-sockets.

The table below shows the configuration of the solder bridges (LBx) and resistors (Rx):

EPROM	Size	LB3	LB4	LB5	LB6	R23	R24	R25	R26	R33	R34
Am29F800 onboard + 2 * Am29F040 on PLCC	512k*16 + 2 * 512k*8	X	-	-	X	X	-	X	-	X	X

X = solder bridge closed or resistor equipped
- = solder bridge is opended or resistor is removed

11.4 Onboard Flash-EPROM in combination with (Flash-) EPROM on PLCC

This chapter describes other special uses of (Flash-) EPROMs on the Module C167CR_2. That means using Onboard-Flash-EPROM in connection with (Flash-) EPROMs on PLCC sockets. **Such configurations should be ordered together with the module.**

Note, that the UART 16C550 has to be removed in case of using the Onboard-Flash in combination with (Flash-) EPROMs on PLCC sockets, because the chip select -CS3 is needed for the Onboard-Flash.

The table on the next page gives an overview about special EPROM equipment.

Onboard Flash-EPROM in combination with (Flash-) EPROM on PLCC-sockets:

EPROM (Manufactors Code)	Type	Size	LB3	LB4	LB5	LB6	R23	R24	R25	R26	R33	R34
Am 29F400 onboard + 2 x 27C010 on PLCC	FE E	256k*16-Bit + 2 x 128k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F400 onboard + 2 x 27C020 on PLCC	FE E	256k*16-Bit + 2 x 256k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F400 onboard + 2 x 27C040 on PLCC	FE E	256k*16-Bit + 2 x 512k*8-Bit	X	-	-	X	-	X	-	X	-	X
Am 29F400 onboard + 2x Am29F010 on PLCC	FE FE	256k*16-Bit + 2 x 128k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F400 onboard + 2 x Am29F040 on PLCC	FE FE	256k*16-Bit + 2 x 512k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F800 onboard + 2 x 27C010 on PLCC	FE E	512k*16-Bit + 2 x 128k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F800 onboard + 2 x 27C020 on PLCC	FE E	512k*16-Bit + 2 x 256k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F800 onboard + 2 x 27C040 on PLCC	FE E	512k*16-Bit + 2 x 512k*8-Bit	X	-	-	X	-	X	-	X	X	-
Am 29F800 onboard + 2x Am29F010 on PLCC	FE FE	512k*16-Bit + 2 x 128k*8-Bit	X	-	-	X	X	-	X	-	X	-
Am 29F800 onboard + 2x Am29F040 on PLCC	FE FE	512k*16-Bit + 2 x 512k*8-Bit	X	-	-	X	X	-	X	-	X	-

X = solder bridge closed or resistor equipped
- = solder bridge is opended or resistor is removed

The CS3 has to be applied to the Onboard-Flash instead of CS0. This is done via opening LB5 and closing LB6. Because CS0 is connected to the PLCC-sockets, the (Flash-) EPROMs on PLCC will be selected after RESET.

11.5 The Module C167CR_2 without UART 16C550

The chip select -CS3 of the UART can also be used for the Onboard-Flash in combination with (Flash-) EPROMs on PLCC-sockets. In this case, -CS0 is applied to the (Flash-) EPROMs and -CS3 to the Onboard-Flash. So, the UART has to be removed.

Removing the UART 16C550 should be done by equipping the resistors R5, R6, R7 and R40 to get EA16, EA17, EA18 and VPP at the connector of the Module C167CR_2.

This option should also be ordered together with the module.

11.6 The Module C167CR_2 with one MByte SRAM

Optional, the Module C167CR_2 can also be ordered with one MByte SRAM instead of 256 kByte SRAM (standard).

11.7 The Module C167CR_2 with CAN driver 82C250

Because of the compatibility to the Module C167CR, the CAN driver 82C250 (U19) is not equipped in the standard configuration. Via the 0Ω resistors R36 and R37, the signals CAN_RXD and CAN_TXD are directly applied to the connector (pin 83 and 115) of the module.

Certainly, you can order the Module C167CR_2 with the CAN driver 82C250. The resistors R36 and R37 will be removed then.

11.8 Further configurations on the Module C167CR_2

The port pins P2.8 and P2.9 of the processor can be connected with the interrupt outputs of the UART and the RTC via the solder bridges LB1 and LB2. LB1 connects -INT_RTC with P2.8 and LB2 connects INT_UART with P2.9.

System startup configurations are made via the resistors R1 - R4, R13, R39 and R41. Through pulling down individual lines of Port 0 to a low level, the default configuration of the processor is changed to the needs of the Module C167CR_2 (see user's manual of Siemens C167CR for a detailed description). The bus configuration (BTYP) for the default address range (BUSCON0) is selected via Port 0 during reset, provided that pin -EA is low during reset.