Ethernet Receive Data FIFO Overflow Workaround for the NS9775

Table of Contents

Ethernet Receive Data FIFO Overflow Workaround for the NS9775

Overview

This application note describes:

- NS9775 Ethernet receive data FIFO overflow errata
- Software workaround for the errata

Description of errata

The Ethernet receiver intermittently locks up in 100 Mbps half-duplex applications due to an overflow in the RX Data FIFO.

The Ethernet Interrupt Status register indicates this condition by setting the RX_OVFL_DATA bit.

Software workaround

Reset the RX Ethernet logic when an RX_OVFL_DATA interrupt is generated. The Ethernet driver uses these steps to recover from the stall condition.

1. Clear the ERX bit in Ethernet General Control Register #1.
2. Clear the ERXDMA bit in Ethernet General Control Register #1.
3. Clear the REXEN bit in MAC Configuration Register #1.
4. Clear the RX_OVFL_DATA bit in the Ethernet Interrupt Status register by writing a 1 to the bit.
5. If packets were received before the stall condition and are waiting to be serviced, service them as usual.
6. Reinitialize the Ethernet receive DMA rings.
7. Reload the RX Buffer Descriptor Pointer registers.
8. Clear the RXINIT bit in the Ethernet General Status register by writing a 1 to the bit.
9. Set the ERX bit in Ethernet General Control Register #1.

10. Set the `ERXINIT` bit in Ethernet General Control Register #1.
11. Wait for the `RXINIT` bit in the Ethernet General Status register to be set.
12. Clear the `ERXINIT` bit in Ethernet General Control Register #1.
13. Set the `ERXDMA` bit in Ethernet General Control Register #1.
14. Set the `RXEN` bit in MAC Configuration Register #1.

The Ethernet receive DMA indexes for all rings are reset to zero by the procedure.

The Ethernet driver's internal variables must be updated accordingly before the driver services any packets after executing this procedure.