- Place C27 close to U1.12
- Place C20 close to U1.37
- Place C29 close to U1.64
- Place C30 close to U1.20
- Place C31 close to U1.31
- Place C32 close to U1.42
- Place C33 close to U1.56
- Place C34 close to U1.50
- Place C35 and C36 close to U1.9
- Place C37 and C38 close to U1.4
- Place C39 and C40 close to U1.49
Notes

1. The FT4232H chip has 4 separate I/O ports. Each of these ports can be set to different modes at any time. Only one mode can be set on a port at a time. All of the ports can be set to serial asynchronous bit-bang, or synchronous bit-bang. Only ports A and B can be set to MP55E mode, which includes SPI, I2C, and JTAG modes. The default state for all of the ports will be UART whenever plugged in. This cannot be changed.

2. The FT4232H chip supports two modes for the SPI clock. The first mode supports speeds from 52 Hz to 5 MHz and follows the equation below. ICD is the clock divisor and must be an integer:

   \[ f = \frac{12 \text{MHz}}{12 \times (1 + \text{ICD})} \]

   The other mode can handle speeds between 460 Hz and 30 MHz and follows the equation below:

   \[ f = \frac{50 \text{MHz}}{2 \times (11 + \text{ICD})} \]

   The MOSI and MISO lines are synchronous with the SPI clock. All of the other GPIO pins are not.