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# NS7520 to NS9210 Migration Guidance

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## Overview

The Digi NS9210 processor is designed to be a pin-compatible replacement for existing NS7520 based hardware designs, allowing customers to easily upgrade their products to a much more powerful processor platform with minimized hardware design effort.

The Digi NS9210 offers speed grades up to 150 MHz, integrated cache, a NIST-compliant 256-bit AES accelerator, Digi's patented dynamic power management, and features such as up to 4 high-speed UARTs, SPI with boot functionality, fast-mode I2C, quadrature decoder, PWM, ten general purpose timers/counters, access to up to 2 Flexible Interface Modules, and a total of 54 multiplexed GPIOs.

This document provides general guidance for customers migrating existing product designs based on the NS7520 processor to the Digi NS9210 processor by outlining the design modification related aspects that need specific attention.

Please also refer to the current revision of the Digi NS9210 Hardware Reference Manual for detailed technical information about the processor and its design characteristics.

## Design Aspects

### Core voltage

The NS7520 requires 1.5V at 125mA max.

The NS9210 requires 1.8V at different current depending on the mode of operation. See table below for examples.

NS9210 Operation	Description	Current Draw @ 1.8V	Comments
<b>"NS7520 Mode"</b>	CPU at 56 MHz running external SDRAM memory test External memory /AHB Bus at 56 MHz No FIM clocks 2 UARTs running Ethernet transmitting and receiving packets	224 mA, 0.403W	May require a higher current rated power source
<b>Full Speed</b>	CPU at 150 MHz running external SDRAM memory test External memory / AHB Bus at 75 MHz Both FIM clocks running at 300 MHz Ethernet transmitting and receiving packets	489 mA, 0.880W	May require a switching power source to reduce heat

Table 1: NS9210 1.8V Current Draw Examples

### Clock source

The NS7520 uses 18.432 MHz.

The NS9210 uses 29.4912 MHz.



*May require a spread spectrum clock to reduce EMI with FIMs enabled.*

### New 3.3V and GND Pins

The NS9210 adds 7 new 3.3V pins, and 5 new GND pins.



*Connecting these pins to 3.3V and GND can improve operating margins and reduce EMI.*

The table below provides an overview of the new pins and the corresponding use on the NS7520.

Pin	NS9210	NS7520	NS7520 Use
<b>C7</b>	GND	BG#	Left open
<b>N12</b>	GND	XTALB1	Tied to GND
<b>R15</b>	GND	XTALB2	Left open
<b>P11</b>	GND	NC	Left open
<b>P13</b>	GND	NC	Left open
<b>D7</b>	+3.3V	BR#	Left open
<b>A8</b>	+3.3V	TS#	External pull-up
<b>P12</b>	+3.3V	Reserved	10-15K to GND
<b>R13</b>	+3.3V	Reserved	10-15K to GND
<b>M11</b>	+3.3V	NC	Left open
<b>R12</b>	+3.3V	NC	Left open
<b>R14</b>	+3.3V	NC	Left open

Table 2: New NS9210 3.3V/GND Pins

## ***Crystal***

The crystal requires a 330R in series with pin K12 (XTAL2). Without this resistor the crystal is being overdriven and could have a shortened life. Crystal overdrive current also causes excessive EMI.

The NS7520 does not need any series resistor.

## ***Write Enable***

The NS7520 has two WE# pins: One for Dynamic, and one for static memory.

NS9210 designs should use pin B3 for all memory types. Pin C6 WE# should be left unconnected.

## ***Boot Flash***

A26 and A27 cannot be used as CS0WE# and CS0OE# to enable boot flash because they initialize as GPIOs.

## ***Memory Bank Selects***

When using 64Mb (2Mx32) SDRAM, A22 and A23 connect to the bank selects on the NS9210.

The NS7520 uses A21 and A22 instead.

## ***PHYs w/MII Signal Bootstrapping***

The MII port boots up in GPIO mode with internal pull-ups active, which conflicts with Ethernet PHYs using MII signals for bootstrap.

To use this specific type of PHY with the NS9210, the PHY needs to be held in RESET until the code sets this port to MII mode with pull-ups disabled. A GPIO with a 2.4K pull-down can be used to control the PHY Reset input.

## ***NS7520 46 MHz Bootstrapping***

Pull-downs on A[3] and A[2]) bootstrap the NS7520 for 46MHz. This will cause the NS9210 to boot at 75MHz.

The NS9210 requires pull-downs A[3], A[2] and A[1] for 44.9MHz.

## ***PLL Bypass***

If the NS7520 design is set for PLL bypass mode with an external oscillator, the PLL will not be bypassed on the NS9210. The NS9210 requires address line 7 to be pulled down.

The NS7520 required the mode pins to be 1,1,1 for PLL bypass.

The NS9210 mode pins at 1,1,1 & 1,1,0 select normal operation with debug enabled.

## ***JTAG Debugger Support***

### **Hard Reset**

The NS7520 maintains the debugger connection when RESET# (hard reset) is active.

The NS9210 does not maintain the debugger connection when RESET# is active. In order to allow maintaining the debugger connection, the new signal SRESET# has been added on pin C8, which is TEA# on the NS7520. For full debugger support pin C8 needs to be connected to the debugger's SRST# pin with a 2.4K pull-up.

### **Download Speed**

The NS9210 can download code from the debugger at faster speeds if the adaptive clocking signal RTCK is brought out to the debugger RTCK input. This new signal is on pin N11, which is a "No Connect" on the NS7520. "No Connect" pins are usually inaccessible on BGA designs. This signal is located on pin 15 of the 20 pin JTAG connector.

In order to work *without* using the RTCK signal, the debugger's adaptive clocking must be disabled and the RTCK pin input to the debugger should be connected to GND.

## ***SPI Ports***

The NS7520 provides two (2) SPI ports.

The NS9210 provides one (1) SPI port.

## ***E14 PORTC0***

There is no interrupt on pin E14 PORTC0 (NS9210 gpio[8]).

## ***New Features***

### **Pin B7**

Pin B7 is BUSY# on the NS7520. The NS9210 adds a new output signal SD\_CKE.

In order to use the new low power modes, which places the SDRAM into self refresh, this signal needs to be connected to the SDRAM's CKE input.

### **Pin D8**

Pin D8 is TA# on the NS7520.

The NS9210 adds a new input signal NS\_TA\_STB. It can be used to add extended wait states for static memory which can be externally terminate the chip select.

### **GPIO: Data[15:0]**

If the memory bus is x16, then Data[15:0] can be used as GPIO.

### **GPIO: MII**

If the MII bus is not used, these eighteen pins can be used as GPIO.

### **GPIO: A[27:24]**

Address lines A[27:24] can be used as GPIO.


### **SPI Boot to SDRAM**

Address line 26 pulled down enables SPI boot to SDRAM from GPIO[11] and GPIO[13:15].



## Commented Schematics

Commented migration schematics are attached to this PDF document.

 *If your version of the Adobe® Reader® does not support PDF file attachments, a standalone PDF file of the commented migration guidance schematics is also available on the Digi support website.*

## Change Log

Revision	Date	Comment
A1	3/20/08	New document