NS7520 Errata

Part number/version: 90000352_L
Release date: February 2006
www.digi.com

For use in conjunction with:
NS7520 Hardware Reference
Part number/version: 90000353_C
Release date: September 2005

Making
DEVICE NETWORKING
easy™

Digi International
11001 Bren Road East
Minnetonka, MN 55343 U.S.A.
United States: +1 877 912-3444
Other locations: +1 952 912-3444
Fax: +1 952 912-4960
www.digi.com/support/
www.digi.com

Online problem reporting:
www.digi.com/support/eservice/eservicelogin.jsp

Contents

NS7520 Errata

This document contains information about NS7520 errata.

How to identify the NS7520

There are three versions of the NS7520, each marked as shown in this sample:

36 MHz version

The part number is constructed as follows:

[*product*][*package*]-[*rev id*]-[*Commercial* or *Industrial*][*speed*]

- 36 MHz version: `NS7520B-1-C36`
- 46 MHz version: `NS7520B-1-I46`
- 55 MHz version: `NS7520B-1-C55`

NS7520 errata

This section lists the known errata for the NS7520, describing each problem and, in most cases, providing a workaround.

Jan 17, 2006

UART CTS-related transmit data errors

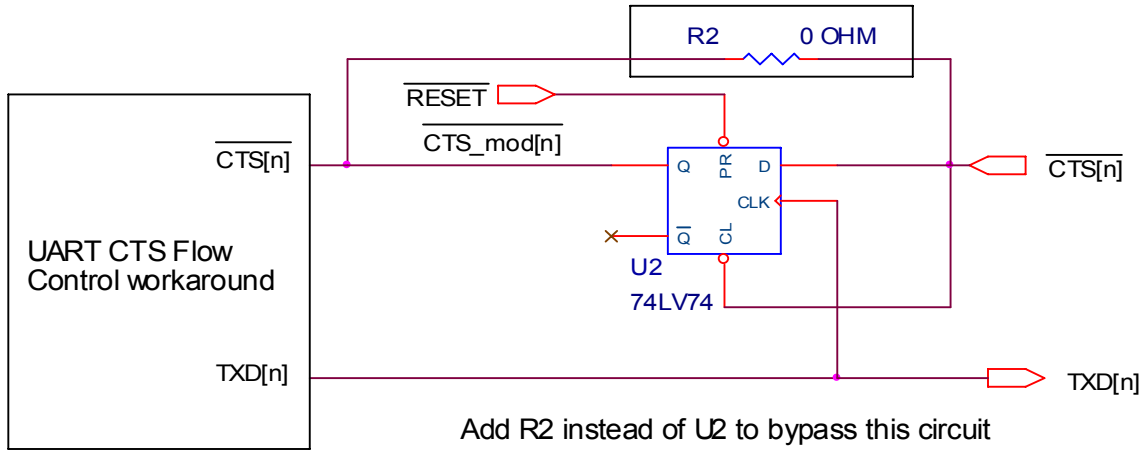
A problem occurs when the CTS flow control signal is de-asserted during the BCLK that begins processing a new character. This problem causes the previous character to be re-transmitted instead of getting the next character from the transmit FIFO.

Software workarounds

- Modify these bits in Serial Channel Control register A:
  - Set the CTSTX bit (bit 23) to 0 to disable hardware-controlled CTSTX.
  - Set the ERXCTS bit (bit 4) to enable the software CTS signal change interrupt.
  - Update the serial transmit ISR to handle the CTS signal change.
- Non-DMA mode: Because FIFO can hold up to eight lines of 4 bytes each, the maximum skid rate will be 32 characters.
- To reduce the maximum skid rate to eight characters, the software is changed to write 1 byte in each line.
- In DMA mode, the skid rate can be up to the number of bytes transmitted in 1 tick.
- The serial monitor thread is changed to handle the missing CTS interrupt.

Hardware workaround

For each UART, externally clock the CTS signal with the Txd_n signal to guarantee that CTS will not be seen de-asserting at the start of a character.



EDO burst errata

The WAIT field in the Chip Select Option register controls the wait states of the first cycle of an EDO burst. The wait states for the secondary cycles are controlled by the BCYC field. Secondary cycles, therefore, are intended to be shorter than the first cycle, for faster transfers.

When a chip select is configured as EDO, the wait states in the secondary cycles are, incorrectly, the sum of the WAIT and BCYC fields, making the secondary cycles longer than the first cycle.

Example

The WAIT field is set to 3 and the BCYC field is set to 1, resulting in 4 wait states in the secondary cycles.

Note: Setting the BCYC field to 0 is not an option because that produces the maximum number of wait states:

```
63 WAIT + 15 BCYC = 78 wait states on the secondary cycles
```

Workaround

Use the Fast Page setting when using EDO DRAM.

Ethernet transmitter considerations

The *NS7520 Hardware Reference* omits the following procedure from Chapter 8, "DMA Controller Module."

Under heavy load, the Ethernet transmitter can, on rare occasions, fail to recover from aborted transmits caused by events such as late collisions and transmit underruns. This situation occurs under the following conditions:

- TXCOLC or TXAUR bits in the Ethernet Transmitter Status register are set to 1.
- Full bit in the current DMA buffer descriptor is set to 1.
- Status field in the DMA buffer descriptor is set to 0.

The transmit operation will not proceed until the condition is corrected.

In general, the problem of transmit underruns can be avoided by running in half duplex rather than full duplex. Late collisions can be eliminated by proper network design; late collisions are caused by too many cascaded levels of hubs, switches, repeaters, and the like.

Correction

To correct an underrun condition, use these steps:

1. Disable the DMA channel by setting the CE bit to 0 in the DMA Control register.
2. Disable the transmit DMA and transmit FIFO by setting the ETXDMA and ETX bits to 0 in the Ethernet General Control register.
3. Initialize the buffer descriptors and DMA buffer descriptor pointer.
4. Enable the transmit DMA and transmit FIFO by setting the ETXDMA and ETX bits to 1 in the Ethernet General Control register.
5. Enable the DMA channel by setting the CE bit to 1 in the DMA Control register.

The transmit DMA now starts again at the beginning. The recovery is implemented in the NET+OS BSP, no data is lost, and there is no other effect on operation.

NS7520 clock speed erratum

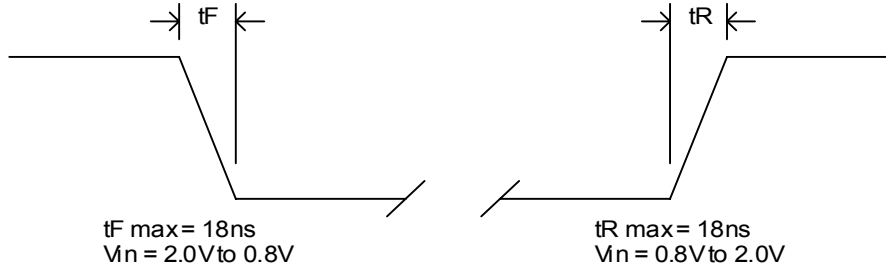
When the NS7520 is configured to use the PLL clock generator, the system clock can come up at 1/2 the configured frequency, or at a higher frequency — usually 64 MHz.

When the PLLTST and BISTEN signals are set high with the SCANEN signal low, the PLL clock generatorshould produce the system clock based on the code it reads on address signals A[4:0]. on occasion, the system clock is either 1/2 the frequency or greater than the configured frequency due to the internal PLL circuitry not being properly reset.

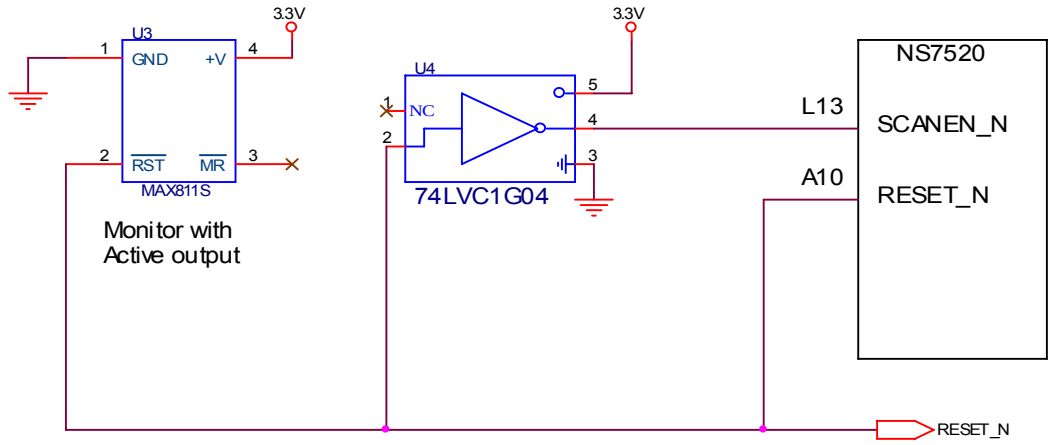
Note: When the PLL is bypassed, PLLTST_N, BISTEN_N, and SCANEN_N all equal a logic "1" and this erratum does not apply.

Workaround

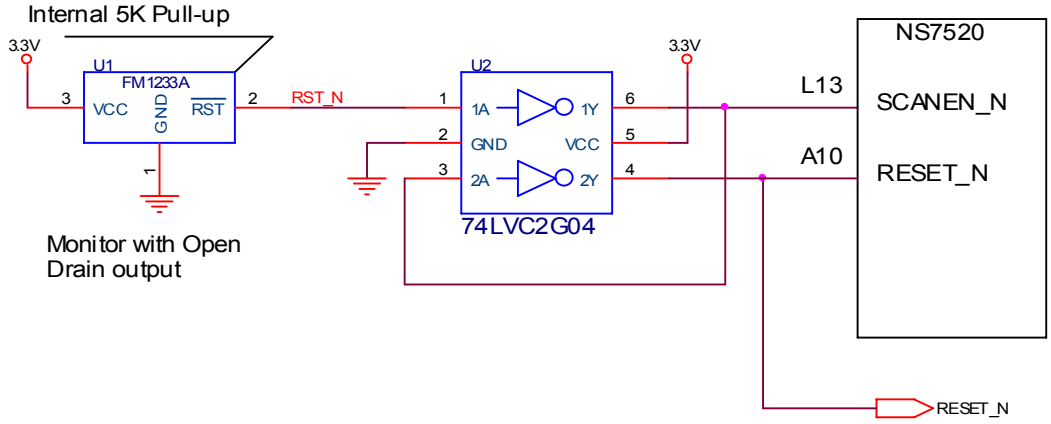
Ensure that the RESET source has adequate fall/rise times and is free from glitches and ringing to prevent 64 MHz or other higher frequencies. This example shows rise and fall timing:



Invert the active LVTTL RESET_N signal and attach it to the SCANEN_N pin to prevent the 1/2 BCLK failure. The maximum delay (inverter propagation delay plus the etch delay) between pins A10 and L13 must be less than 8ns. This next example shows the SCANEN_N inverter with active TTL monitor:



Most open drain power monitors require a speedup circuit in order to meet the fall/rise timing. This next example shows RESET speed up with open drain monitor:



An external RESET_N source with a rise time exceeding 18ns (0.8V to 2.0V) should use a Schmitt trigger speedup circuit such as 74LVC2G14.

SPI slave mode errata

SPI slave modes are non-functional. SPI slave logic is unable to sample or drive data on the correct clock edges. This causes byte mismatches.

Workaround

None.

SPI maximum bit rate

The *NS7520 Hardware Reference* (90000353B, released January 2003) incorrectly lists the serial port maximum bit rate in SPI as SYSCLK/8. The correct value is SYSCLK/6.

Correction

This error will be corrected in the next release of the *NS7520 Hardware Reference*.

SPI Channel Bit-Rate register bit definition

The *NS7520 Hardware Reference* (90000353B, released January 2003) incorrectly lists bit D21 in the SPI Channel Bit-Rate register table as `Reserved`. Bit D21 is `CLOCK INVERT`, and should be defined as follows:

Bit:	D21	
Access:	R/W	
Mnemonic:	CLKINV	
Reset:	0	
Description:	0	Initial value of the clock signal is low.
	1	Initial value of the clock signal is high.

Correction

This error will be corrected in the next release of the *NS7520 Hardware Reference*.

Statistics gathering

The NS7520 does not support Ethernet statistics gathering. The *NS7520 Hardware Reference*, however, does reference statistics in three locations:

- Page 136, Figure 20
- Page 140, "Basic MAC module features"
- Page 166, Table 67 (MAC Configuration register bit description, D01).

Correction

The errors will be corrected in the next release of the *NS7520 Hardware Reference*.

PAD operation

The PAD operation table (EFE configuration) in the *NS7520 Hardware Reference* incorrectly specifies the **PADEN** value as 0 for the "Pad to 60 bytes; append CRC" option. The correct value is 1.

Workaround

None.

DMA bandwidth settings

The DMA bus bandwidth field (bits 29:28 in the DMA Control register) determine how often the DMA channel can arbitrate for access to the bus. Settings for this field include 100%, 75%, 50%, and 25%. This table shows the actual operation.

DMA code	What's in manual	Actual operation
00	100% (no limit): The DMA channel can arbitrate each time.	100% (no limit): The DMA channel can arbitrate each time.
01	75%: The DMA channel can arbitrate 3 out of 4 times.	100% (no limit): The DMA channel can arbitrate each time.
10	50%: The DMA channel can arbitrate 2 out of 4 times.	50%: The DMA channel can arbitrate 2 out of 4 times.
11	25%: The DMA channel can arbitrate 1 out of 4 times.	50%: The DMA channel can arbitrate 2 out of 4 times.

Workaround

None.

Correction

This error will be corrected in the next release of the *NS7520 Hardware Reference*.

Error in "No Connect" pin terminations

Table 9: "No Connect" pins in the *NS7520 Hardware Reference* erroneously advises connecting pins R13, P12, and N12 directly to V_{CC}. This can cause the NS7520 to draw excessive V_{CC} current, *at times* following RESET, in the range of 120 ma. This will cause the case temperature to rise above normal, but exhibits no operational failures.

Workaround

1. *For existing designs:* Cut the pin R13, P12, and N12 traces to the V_{CC} supply connection. This will "float" pins R13, P12, and N12. It is advisable to modify the PCB to add two pulldown resistors and one GND, as recommended next for new designs.
2. *For new designs:* Add individual 15K ohm pulldowns to GND on R13 and P12. Tie N12 to ground. (A 15K ohm pulldown is the recommended value; 10–20K ohms is acceptable.)

Note: On designs that have implemented 10 to 20K ohm pullups instead of pulldowns on R13 and P12 pins or GND on N12, no action is required. This method of termination limits the increase of V_{CC} current, *at times* following RESET (333uA with 10K ohm pullup or 165 uA with 20K ohm pullup).

Correction

Table 9 in the *NS7520 Hardware Reference* will be corrected in the next revision.

Serial port error in 7-bit mode

The NS7520's serial ports do not function correctly when configured in the 7-bit mode. The 7-bit transmitter will transmit 8-bit data, and the data in the receive buffer will be incorrect. The other modes — 8-bit, 6-bit, and 5-bit — all function correctly.

Workaround

None. Use the 8-bit, 6-bit, or 5-bit modes only.

SDRAM 256 MB mask failure

The NS7520 chip select does not generate the required precharge commands if a value larger than 128 MB is written in the Chip Select Option register mask word. In particular, if the SDRAM is located at 0–256M and one read is done at address `0x400` and another read is done at address `0x0`, there is no precharge for the read at address 0.

Workaround

Mask size `0xF0000` (256 MB) should not be used.

Erroneous timeouts when loading timer

There can be two erroneous timeouts when the timer is first loaded.

Workaround

In most cases, no workaround is required because the error averages out over many readings. The problem can become critical if you set the timer to a large value, such as four hours. A workaround for this situation is to program the timer to timeout twice, with a small value such as 4μ, then load the larger value.

Example

```
0xffb00010 = 80000001;
           Wait for the first TIP bit. Reset the TIP bit.
           Wait for the first TIP bit. Reset the TIP bit.
0xffb00010 = 80ffffff;
```

In this way, the two erroneous timeouts will occur with a small value, and the large value can then be set.

Note: Toggling TE (timer enable) to disable and re-enable the timer does not eliminate this issue.

Station Address Logic: Multicast and broadcast packet filtering

The station address logic (SAL) in the MAC receiver does not filter multicast and broadcast packets in a predictable manner.

Workaround

Program the Station Address Filter register (SAFR) fields as shown:

Mnemonic	Bit	Value	Description
PRO	D03	0	Disable promiscuous mode
PRM	D02	1	Accept all multicast packets
PRA	D01	0	Disable multicast hash table
BROAD	D00	1	Accept all broadcast packets

If filtering of multicast and broadcast packets is required, it must be provided by software.

Station Address Logic: Unicast packets

The station address logic (SAL) in the MAC receiver does not compare the first byte of the Ethernet destination address against the OCTET6 value in the Station Address Register 3 (SA3) for unicast packets. As such, the SAL does not reject unicast packets with mismatches only in this field.

The first byte of the Ethernet destination address is the first byte of the *organizationally unique identifier* (OID) portion of the address. Mismatches that occur only in this byte of the Ethernet destination address are rare.

Workaround

In most cases, upper level protocols such as TCP/IP check the software level address of the packets and reject any packets not sent to the proper address. Otherwise, software must provide a check of this byte of the address.

Corrupt Ethernet receive packets

Under extremely rare conditions, packets passed between the Ethernet MAC and the receive FIFO have a packet word transferred twice. The last word of the packet is then dropped. For those Ethernet packets where the higher level protocol does not provide a checksum, corrupted data might be passed to the application.

The problem frequency has been measured at Digi. Tests have shown frequency at one in 20 million for large packets (1518 bytes) and approximately one in 10-500 million for small packets (64 bytes).

Workaround

Using standard protocols such as TCP/IP or UDP with checksum selected, bad packets are discarded by the stack. Retransmission is requested, as appropriate, for the bad packets. Note, however, that implementing the checksum results in latency and performance degradation.

For protocols that do not have built-in error checking, the Ethernet driver provides a software workaround. You can enable an `#ifdef` statement to perform a software checksum. Go to the support website page and look for the application note called *Porting Ethernet Software CRC to NET+OS 5.0, 5.1, and 6.0*.

Transmit buffer closed bit is not functional

The transmit buffer closed (TXBC) bit, D01, in Serial Status Register A (Serial Controller module) does not work as described.

Workaround

To determine when the last character has been transmitted, use the software workaround for the mode you are using:

Interrupt mode:
There are three options in interrupt mode:

1. Waiting
   - If the FIFO was filled using byte writes, wait 9 character times.
   - If the FIFO was filled using word writes, wait 33 character times.
2. Polling TXEMPTY

   Poll TXEMPTY (bit 0) in Serial Channel Status Register A. When the bit indicates empty, allow 1 character time to let the last character exit the shift register.
3. Using TXHALF interrupt

   You can use this method when filling the FIFO using word writes (32-bit transfers).

   Enable the TXHALF interrupt by setting bit 2 in Serial Channel Control Register A. When this interrupt occurs, it indicates that there are no more than 16 bytes remaining in the FIFO. Once it occurs, wait 17 character times — 16 plus 1 character time to allow the last character to exit the shift register.

DMA mode:
Wait 33 character times after receiving the DMA complete interrupt.

Transmit FIFO timing issue

When transmitting characters from the FIFO, you must be sure each character is shifted out before the next character is processed. Otherwise, the first clock and data bit of the new character can be corrupted.

Workaround

Use the software workaround for the mode you are using:

Interrupt mode:

For all but the first character, check the TXEMPTY bit (D00 in the Serial Status Register A).

- If the TXEMPTY bit is not set, write the next character within 1 character time.
- If the TXEMPTY bit is set, wait 1 character time plus 1 bit time before writing the next character.

DMA mode:

You should not have a problem with this issue when working in DMA mode.

External use of TA_ and TEA_

Note these issues for TA_ and TEA_:

- **TEA_:** Externally generated TEA_ burst cycles can cause failures.
- **TA_:** External TA_ can be used only in single cycle mode, to terminate chip selects with 8, 16, and 32 bus widths.

Workaround

The TA_ signal in the NS7520 must be synchronized with BCLK, and last for one BCLK.

The internal TA synchronizer settings must be as shown:

- Chip Select Option Register B: SYNC — 1 stage (01)
- System Control register — BSYNC: 1 stage (00)

Both TA_ and TEA_ should have external 820 ohm pullups.

Note: The external device never drives TEA_.

Digi International
11001 Bren Road East
Minnetonka, MN 55343 U.S.A.
United States: +1 877 912-3444
Other locations: +1 952 912-3444
Fax: +1 952 912-4960
www.digi.com/support
www.digi.com

Online problem reporting:
www.digi.com/support/eservice/eservicelogin.jsp