NET+50/20M Jumpers and Components

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NET+50 Jumpers and Components Guide

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Contents

Using This Guide

Review this section for basic information about this guide, as well as for general support contact information.

About this guide

This guide provides information about the jumpers and components of the NET+50 development board. The NET+50, part of the Digi NET+ARM line of SoC (System-on-Chip) products, supports any type of high bandwidth application in Intelligent Networked Devices.

The NET+ARM chip is part of the NET+Works integrated product family, which includes the NET+OS network software suite.

Who should read this guide

This guide is for hardware developers, system software developers, and application programmers who want to use the NET+50 for development.

To complete the tasks described in this guide, you must:

- Understand the basics of hardware and software design, operating systems, and microprocessor design.
- Understand the NET+50 architecture.

What's in this guide

This table shows where you can find information in this guide:

To read about	See
A description of the NET+Works development board hardware	Chapter 1, "Hardware Description"
The NET+50 board schematics	Chapter 2, "Schematics"
The bill of materials (BOM) for the NET+50 development board	Chapter 3, "Bill of Materials"

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
bold, sans serif type	Menu commands, dialog box components, and other items that appear on-screen.
Select **Menu → option**	Menu commands. The first word is the menu name; the words that follow are menu selections.
`monospaced type`	Filenames, pathnames, and code examples.

Related documentation

- For information about the chip you are using, see the *NET+50 Hardware Reference*.
- For information about third-party products and other components, review the documentation CD-ROM that came with your development kit.

Documentation updates

Digi occasionally provides documentation updates on the Web site.

Be aware that if you see differences between the documentation you received in your NET+Works package and the documentation on the Web site, the Web site content is the latest version.

Customer support

To get help with a question or technical problem with this product, or to make comments and recommendations about our products or documentation, use the contact information listed in the table shown next.

For	Contact information
Technical support	Telephone: 1 877 912-3444/ 1 952 912-3456 Fax: 1 952 912-4960
Documentation	techpubs@digi.com
Digi home page	www.digi.com/support/eservice/eservicelogin.jsp
Online problem reporting	www.digi.com/problemreporting.jsp

Hardware Description

CHAPTER 1

This chapter provides a hardware description of the NET+Works development board. In addition, this chapter describes how to configure the base address for each chip select, DIP switches, and the 1284 parallel port and ENI interfaces.

The board is identifiable by this information:

- **Market name.** NET+Works Development Board
- **Part number.** 6127030
- **Test reference.** S2NCCTP

The NET+50 consists of a 208 plastic-quad-flat-pack (PQFP) package and a 208 ball-grid-array (BGA) package. A high-performance, highly-integrated 32-bit chip, the NET+50 is designed for use in intelligent network devices and Internet appliances.

Features of the development board

The NET+Works development board provides these basic features:

- 44.3 MHz NET+50 (BGA).

  The NET+50 BGA development board supports applications using the NET+50 QFP processor.
- 18.432 MHz crystal, with option for external oscillator.
- ARM JTAG ICE port.
- Six LED indicators: two each on PORT C, PORT B, and the Ethernet connector.
- 2 ASYNC 1 Mbps serial ports, one with RS485 option, user selectable.
- 10/100BaseT Ethernet port.
- 8Kx8 EEPROM, expandable to 32Kx8.
- Serial EEPROM standard (64K, 8192x8, SPI part on GPIO pins).
- 16Mb DRAM.
- 2MB flash, expandable to 16 MB.
- MIC Port (GPIO, IEEE1284, ENI) interface connector.
- Bootstrap configuration DIP switches.
- Expansion board plugs. All NET+ARM bus signals are brought out.
- TEK Mictor headers for logic analyzer connections.
- Large breadboard area.

Chip select configuration

The peripheral devices are connected to specific chip selects on the NET+ARM chip.

The base address for each chip select must be configured using NET+ARM internal registers, as listed in this table:

Chip select	Peripheral	Maximum size
CS0	Flash	16 MB
CS1	SDRAM	16 MB
CS2	Expansion connector	256 KB
CS3	Parallel EE (default) or expansion connector	32 KB (default) or 256 KB
CS4	Expansion connector	256 KB

Table 1: Chip select configuration

Jumpers and single DIP switch SW2

This table defines the jumpers and DIP switch designations:

Jumper	Purpose
JP1	Serial port B 232 = 1-2 (default); 485 = 2-3
JP2	Serial port B 232 = ON (default); 485 = OFF (on a single pin only)
SW2	Serial port B 232 = 1-4 ON, 5-8 OFF (default); 485 = 1-4 OFF, 5-8 ON
P5-P6	x16 vs x 32 bit SDRAM configuration - SDRAM = x32 (default)
P7-P9	x16 vs x 32 bit flash configuration - flash = x16 (default)

Table 2: Jumpers and DIP switches

Connectors

This table defines the connectors and their designations:

Reference number	Type	Purpose
J1/J2	Mini/din jack	Power connector - 5 pin din populated
J3	RJ45 MAG-jack	10/100 BT Ethernet with LEDs
J4-8	Mictor 38 pin	TEK configured emulator headers
P1	DB9 male	Serial port A RS232, 1 Mbps, full modem support
P2	DB9 male	Serial port B RS232, 1 Mbps or RS485
P3	Header 2x7	ARM ICE port
P4	Header 1x6	Manufacturing test plug
P10	Header 50 pin	MIC port interface - IDC or PCB to PCB
P11	Header 60 pin	Expansion interface D31:16 - IDC or PCB to PCB
P12	Header 60 pin	Expansion interface D15:00 - IDC or PCB to PCB

Table 3: Connectors

This information applies to P10, P11, and P12:

- Mating connectors:
  - Nanoflex high density connectors
  - Yamaichi (search for part number or nfs); http://www.yamaichi.us/
- PBC socket:
  - P10 (change 50 to 60 for P11-P12)
  - nfs-50-1314xx
- ICD socket with strain relief:
  - P10 (change 50 to 60 for P11-12
  - nfs-50A-0111

DIP switches

A group of four 8-position DIP switches is provided for:

- Configuring the NET+ARM
- Selecting Write or Read enable
- Selecting MIC port: Either ENI/DPO or IEEE1284 or GPIO modes

The tables in this section give details about each switch.

In all cases, normal = default position.

Switch 5

Position	Function	Off	On
1	PULINT	Normal	ENI pulsed interrupt out
2	EPACK	Normal	ENI flow control = ACK*
3	Reserved	Normal	Reserved
4	DMAE	Normal	ENI DMA lines enabled
5	I_0C	Normal	ENI interrupt = TTL
6	DINT2	Normal	ENI pulsed interrupt in
7	WR_OC	Normal	ENI wait/ACK = TTL
8	PSIO	Normal	Enable PSIO ENI mode

Table 4: Switch 5

Switch 6

Position	Function	Off	On
1	Reserved	Normal	32-bit BUS for NET+12
2 GEN_ID9	ID0	Normal	Factory default
3 GEN_ID10	ID1	Normal	Manufacturing test

Table 5: Switch 6

Position	Function	Off	On
4 GEN_ID11	ID2	Normal	Spare
5 GEN_ID12	ID3	Normal	Parallel ports bit 0
6 GEN_ID13	ID4	Normal	Parallel ports bit 1
7 GEN_ID14	ID5	Normal	Force download mode
8 GEN_ID15	ID6	Media type bit 0	Normal MII

Table 5: Switch 6

Switch 3

Position	Function	Off	On
1 GEN_ID16	ID7	Media type bit 1	Normal MII
2 GEN_ID17	ID8	Serial ports bit 0	Normal two
3 GEN_ID18	ID9	Serial ports bit 1	Normal two
4 GEN_ID19	ID10	Normal	Spare
5	PCM0	MIC mode bit 0	Normal GPIO
6	PCM1	MIC mode bit 1	Normal GPIO
7	PCM2	MIC mode bit 2	Normal GPIO
8	CS00	Normal	CS0 boot

Table 6: Switch 3

Switch 4

Position	Function	Off	On
1	CS01	Normal	CS0 32 bit flash boot
2	EARB	Normal	External bus arbiter
3	ARMD	Normal	ARM disable

Table 7: Switch 4

Position	Function	Off	On
4	LEND	Normal	Little Endian
5	FWRITE	Flash write disable	Normal
6	FRREAD	Flash Read disable	Normal
7	SP7	Normal	Spare (NC)
8	SP8	Normal	Spare (NC)

Table 7: Switch 4

Expansion plugs

The two 60-pin plugs bring out the entire NETARM system bus, including ports A:C. Some signals have on-board use, but option resistors allow even these to be brought out. If a 16-bit data bus is required, only P11 needs to be attached. Devices that interface to this connector must have 3V signaling levels. The inputs to the NET+ARM are not 5V-tolerant.

The P11 expansion plug is a 16 bit bus; the P12 expansion plug provides the additional 16 bits for a 32 bit bus.

This table shows the functions for P11:

Signal name	Function
VCC or 3.3V	5.0V @ 500 mA or 3.3V 300 mA (includes both P11+ P12)
A7:0	Address lines (up to 256 KB)
D31:16	Data lines upper
BE3:2	Byte enable lines upper
CS2*, CS4*	Chip selects
CS3*	Chip select used by parallel EE (R71 isolates)
OE*, WE*, RW*	Chip select direction
CASI*	Used by SDRAM

Table 8: P11 functions

Signal name	Function
RESET*	Hardware reset input to NETARM
PORTA7:0	Used on board (R57, 58, 59, 14, 143,34,26,25 isolates)
PORTB7:0	Used on board (R29, 39, 31, 80, 16, 20, 17, 21 isolates)
PORTC7, PORTC5	Used on board (R121 and R90 isolates)

Table 8: P11 functions

This table shows the functions for P12:

Signal name	Function
VCC or 3.3V	5.0V @ 500V or 3.3V 300mA (includes both P11+ P12)
A27:8	Address lines (up to 256MB)
D15:0	Data lines lower
BE1:0*	Byte enable lines lower
TA*, TEA*	Bus control
TS*	No connect
BR*, BG*, BUSY*	No connect
PORTC6 or CAS0*	Used on board (R162+113 or R161 selects or isolates)
PORT4:3	Used on board (R122, 144 isolates)
PORTC2	Used on board (R163+5 or R164 selects or isolates)
PORTC1	Used on board (166+7 or R165 selects or isolates)
PORTC0	Used on board (R79 isolates)

Ethernet interface

The 10/100 version of the development board provides a full-duplex 10/100Mbit Ethernet interface using the Intel (formerly Level1) 3V PHY in a BGA package, which uses the standard MII interface.

The RJ45 connector is integrated with the isolation transformer, EMI filter components, link, and receive LEDs.

You also can use the MII interface to determine the current Ethernet link status. Change of link status can cause an interrupt on IRQ0*.

The Intel 3V PHY Reset* signal can be connected to the NET+ARM PORTB4 GPIO signal or hardware reset using option resistors. The PORTB4 (R80) signal can be driven low to provide a hard reset to the PHY. Current population uses hardware reset (R75).

The Intel PHY PHYINT* signal is connected to the NET+ARM PORTC0 IRQ0* signal. The PORTC0 input can be configured to generate an interrupt on the high to low transition of PHYINT*. Using this interrupt is not a requirement.

MIC (IEEE1284, GPIO, and ENI interfaces)

You can configure the development board to operate using either the IEEE1284 parallel ports, GPIO mode, or the ENI interface. You can use one interface at a time.

1284 parallel port ENI interface

External glue logic is required to use the IEEE1284 interface. See the IEEE1284 section in the Hardware Reference Guide. This is a multiplexed interface that uses one 74FCT16646 per port. All inputs require 5V to 3.3V translation.

GPIO interface

There are 16 I/O pins and 16 input only pins. Inputs can be set to cause an interrupt or can be polled. Most outputs have 2ma drive with the exception of PORTF7, which has 8ma drive. Signals PBD15:8 should have no connections in GPIO mode.

ENI/DPO interface

If you use a cable to connect to connector P10, the cable should be three inches or shorter. A data buffer may be required. This buffer can be controlled by ENI signals PBRW*(DIR) and PEN*(OE*).

Protype breadboard area

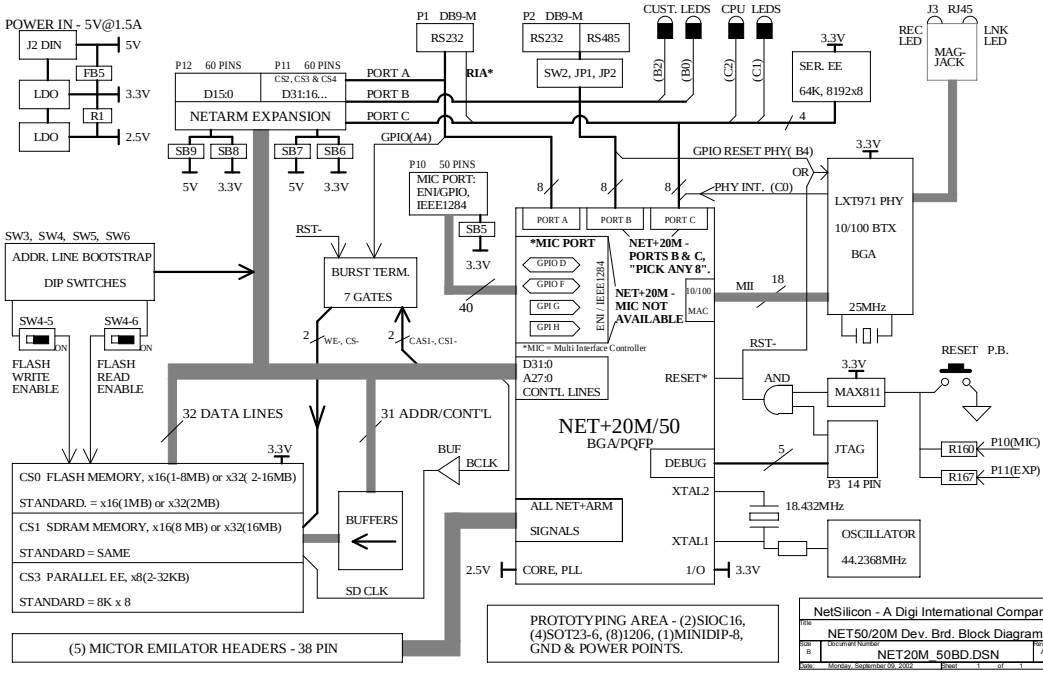
This area provides space for:

- 2 SIOC16 or SIOC14 ICs
- 4 SOT23-6, SOT23-5, SOT23-4...
- Discretes in the 1206 package
- Minidip 8 pin through hole IC
- GND connection points
- 3.3V connection points

Schematics

CHAPTER 2

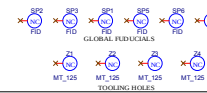
This chapter provides the schematics for the NET+Works development board.


POWER IN - 5V@1.5A
J2 DIN
5V
FB5
LDO
3.3V
R1
LDO
2.5V
P12 60 PINS
P11 60 PINS
CS2, CS3 & CS4
D15:0
D31:16...
NETARM EXPANSION
PORT A
PORT B
PORT C
RIA*
P1 DB9-M
RS232
P2 DB9-M
RS232
RS485
SW2, JP1, JP2
CUST. LEDS
CPU LEDS
(B2)
(B0)
(C2)
(C1)
3.3V
SER. EE
64K, 8192x8
4
J3 RJ45
REC LED
LNK LED
MAG-JACK
SB9
SB8
SB7
SB6
5V
3.3V
5V
3.3V
GPIO(A4)
GPIO RESET PHY(B4)
OR
PHY INT. (C0)
3.3V
LXT971 PHY
10/100 BTX
BGA
25MHz
P10 50 PINS
MIC PORT:
ENI/GPIO,
IEEE1284
8
8
8
PORT A
PORT B
PORT C
*MIC PORT
GPIO D
GPIO F
GPI G
GPI H
ENI / IEEE1284
NET+20M - PORTS B & C, "PICK ANY 8".
NET+20M - MIC NOT AVAILABLE
10/100
MAC
MII
18
*MIC = Multi Interface Controller
SW3, SW4, SW5, SW6
ADDR. LINE BOOTSTRAP
DIP SWITCHES
SW4-5
SW4-6
ON
FLASH WRITE ENABLE
FLASH READ ENABLE
RST-
BURST TERM.
7 GATES
2
WE-, CS-
2
CAS1-, CS1-
SB5
3.3V
40
D31:0
A27:0
CONT'L LINES
RESET*
RST-
AND
3.3V
MAX811
RESET P.B.
32 DATA LINES
31 ADDR/CONT'L
NET+20M/50
BGA/PQFP
DEBUG
5
JTAG
P3 14 PIN
R160
P10(MIC)
R167
P11(EXP)
3.3V
BUF
BCLK
CS0 FLASH MEMORY, x16(1-8MB) or x32(2-16MB)
STANDARD. = x16(1MB) or x32(2MB)
CS1 SDRAM MEMORY, x16(8 MB) or x32(16MB)
STANDARD = SAME
CS3 PARALLEL EE, x8(2-32KB)
STANDARD = 8K x 8
BUFFERS
ALL NET+ARM
SIGNALS
XTAL2
18.432MHz
XTAL1
OSCILLATOR
44.2368MHz
SD CLK
2.5V
CORE, PLL
1/O
3.3V
(5) MICTOR EMILATOR HEADERS - 38 PIN
PROTOTYPING AREA - (2)SIOC16, (4)SOT23-6, (8)1206, (1)MINIDIP-8, GND & POWER POINTS.
NetSilicon - A Digi International Company
NET50/20M Dev. Brd. Block Diagram
NET20M_50BD.DSN
Monday, September 09, 2002

CONFIDENTIAL MATERIAL TO NetSilicon - A Digi International Company

NOTES:

1. ALL RESISTORVALUES ARE IN OHMS AND IN THE 0603SIZE UNLESS OTHERWISE NOTED
2. ALL RESISTORVALUES ARE 5% UNLESS OTHERWISE NOTED
3. ALL CAPACITORS ARE RATEDIN pFARADS AND IN THE 0603 SIZE UNLESS OTHERWISE NOTED
4. ALL CAPACITORS ARE RATEDAT 16 VDC ORHIGHER UNLESS OTHERWISE NOTED
5. L AST USED:



N20M50Bga

DEVELOPMENT BOARD

BOARD REVISIONS

04/18/02 1951000 REV A
07/23/02 1951001 REV B

BOARD REV NOTES

REB B PCB incorperates REV B SH.13 correction

SHEET REV NOTES

Sh.02 Rev B: Updates PORT Descriptions
Sh.04 Rev B: Updates Table 1 C1 to C22
Sh.08 Rev B: Updates Note for RTSB* 1K pull-down.
Sh.09 Rev B: Updates Note for TXD3:0 Resistors - Sh.01 to Rev C
Sh.12 Rev B: Changes 2.5 regulator Capacitor C10 from 4.7 to 10uF LESR
Sh.13 Rev B: Swapped mis-connected 3.3V & GND pins on U16

SHEET DESCRIPTION

SH. #	REV.	DESCRIPTION
1.	C	Cover Sheet
2.	B	Port & Chip Select Information
3.	A	NETARM BGA & BCLK Buffer
4.	B	Emulator Hdrs., Jtag, & Addr. Buffers
5.	A	Flash, Parallel & Serial EE Memory
6.	A	SDRAM Memory
7.	A	1Mbps Serial Port A(1)
8.	B	1Mbps Serial Port B(2) or RS485
9.	B	Ethernet Front End; 10/100BaseTX
10.	A	ENI/GPIO Port
11.	A	System Bus Expansion Conn. & Dipswitches
12.	B	Power Supply, Breadboard Area, & LEDs
13.	B	NETARM PQFP

REF SCH1951001

DESIGNER: Don Stone

NetSilicon - A Digi International Company, Waltham, MA

Title: NET+ARM 20M/50 COVER SHEET

Size | Document Number: n20m50b01.SCH | Rev: C

Date: Thursday, September 05, 2002 | Sheet 1 of 13

Port A - High Speed RS232 Serial Port with Modem Support

0 DCD* Serial port 1
1 CTS* Serial port 1
2 DSR* Serial port 1
3 RxD Serial port 1
4 Burst Terminate (0 Outside arms burst terminate fix)
5 RTS* Serial port 1
6 DTR* Serial port 1
7 TxD Serial port 1
All 8 bits go to Expansion Connector and can be disabled for off-board use.

Port B - High Speed RS232 Serial Port or RS485

0 General Purpose LED, (0 Outside = LED on)
1 CTS* Serial port 2
2 General Purpose LED, (0 Outside = LED on)
3 RxD Serial port 2/RS485 Input
4 Reset PHY, (0 Outside = reset. Board is Strapped for Hardware RESET)
5 RTS* Serial port 2/ RS485 Driver Enable, (1 Outside = Enable)
6 DTR* Serial port 2/ RS485 Receiver Enable, (0 Outside = Enable)
7 TxD Serial port 2/ RS485 Output
All 8 bits go to Expansion Connector and can be disabled for off-board use.

Port C - Serial EE Memory

0 Interrupt from PHY (input)
1 CPU LED Green, (0 Outside = LED on)
2 CPU LED Yellow, (0 Outside = LED on)
3 Serial EE Clock (output) or AMUX
4 Serial EE (data input)
5 Serial EE (data output)
6 RIA* Serial port 1(Or Serial EE Clock output)
7 Serial EE chip select, (0 Outside = selected)
All 8 bits go to Expansion Connector and can be disabled for off-board use.

For NET+20M to NET+20UM migration only eight(8) of the sixteen(16) combined PORTB and PORTC pins should be used.

Chip Selects

CS0 Flash Memory, x16 or x32, 1-16Mbytes
CS1 SDRAM Memory, x16 or x32, 8-16Mbytes
CS2 Spare to Expansion Connector
CS3 Parallel EE Memory & to Expansion Connector
CS4 Spare to Expansion Connector

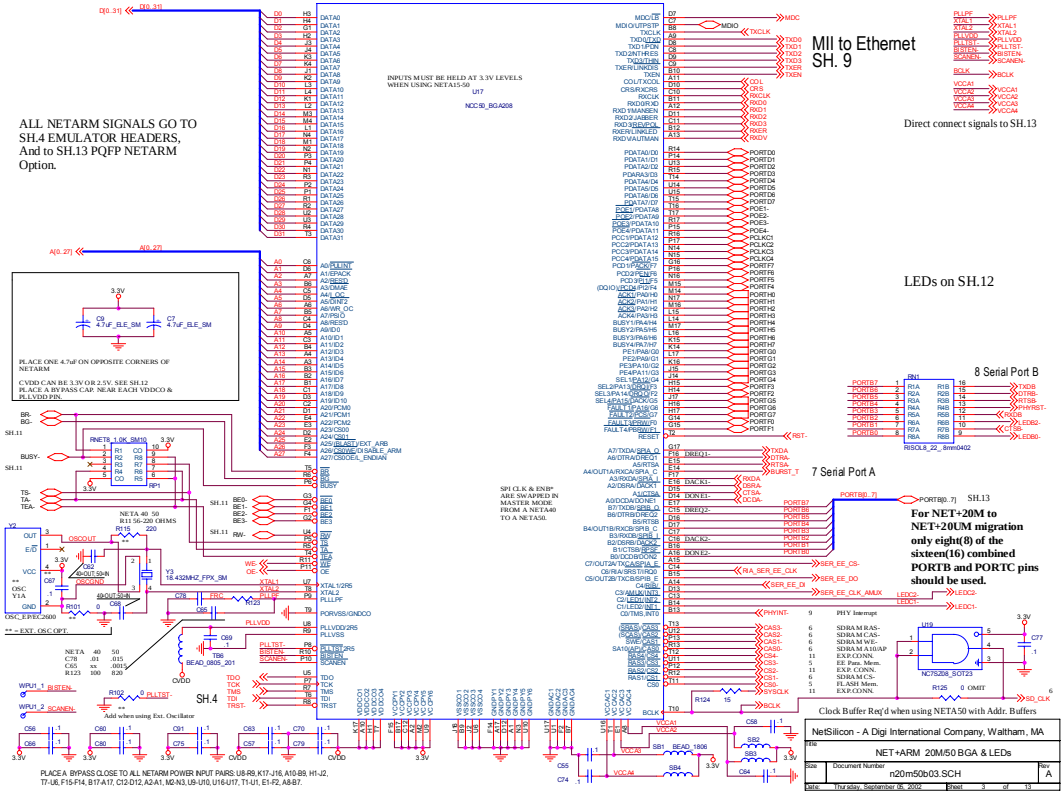
Flash Write and Read are separately controlled by dipswitch

Larger SDRAM Support can be done on Daughter Board. CS1 can be disabled on board.

ENI Port (NET+50 Only)

All Supported GPIO's go to ENI Connector
Supports ENI mode (Data Buffer if required, can be added on daughter board)

NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM 20M/50 Port & Chip Select Information		
Size: B	Document Number: n20m50b02.SCH	Rev: B
Date: Thursday, September 05, 2002	Sheet 2 of 13	


ALL NETARM SIGNALS GO TO SH.4 EMULATOR HEADERS, And to SH.13 PQFP NETARM Option.
INPUTS MUST BE HELD AT 3.3V LEVELS WHEN USING NETA15-50
MII to Ethernet SH. 9
Direct connect signals to SH.13
LEDs on SH.12
8 Serial Port B
7 Serial Port A
SH.4
SH.13
For NET+20M to NET+20UM migration only eight(8) of the sixteen(16) combined PORTB and PORTC pins should be used.
Clock Buffer Req'd when using NETA50 with Addr. Buffers
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM 20M/50 BGA & LEDs
n20m50b03.SCH
Thursday, September 05, 2002

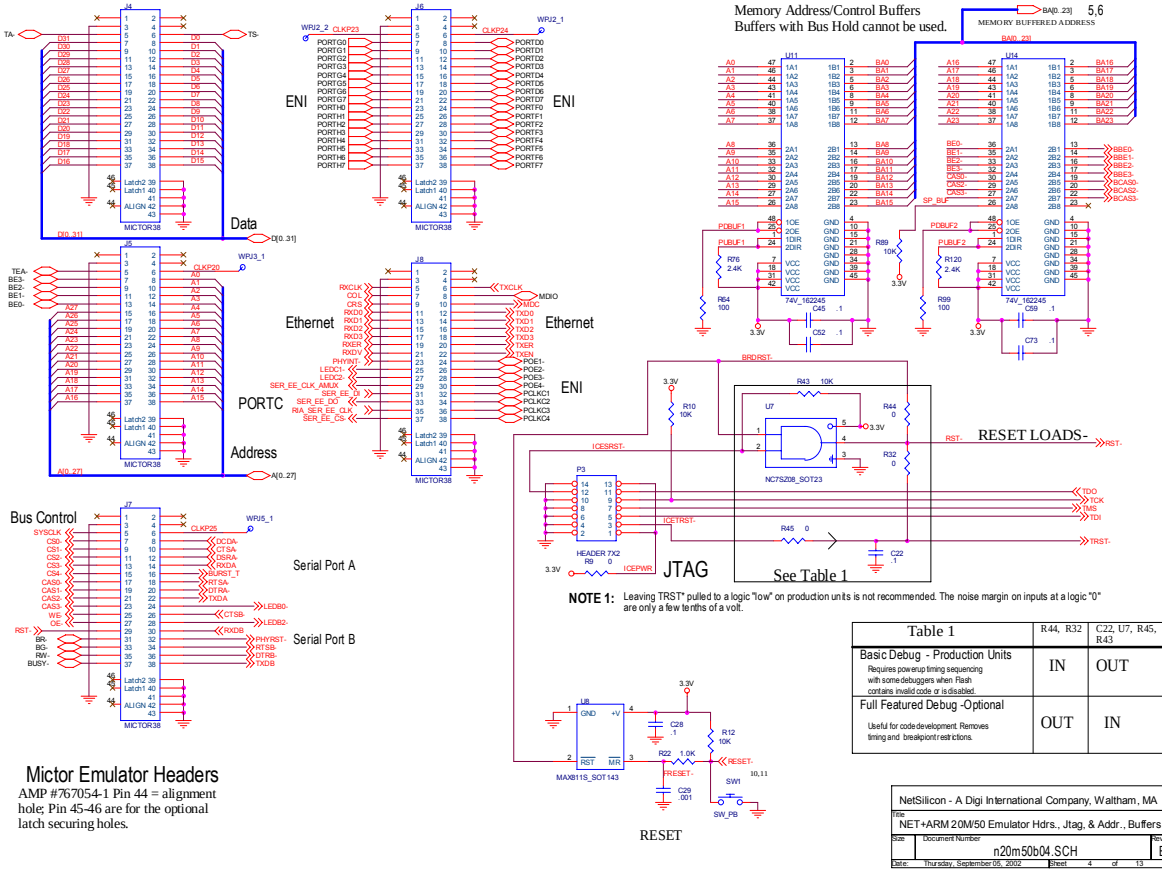


Table 1	R44, R32	C22, U7, R45, R43
Basic Debug - Production Units Requires powerup timing sequencing with some debuggers when Flash contains invalid code or is disabled.	IN	OUT
Full Featured Debug -Optional Useful for code development. Removes timing and breakpoint restrictions.	OUT	IN

Mictor Emulator Headers

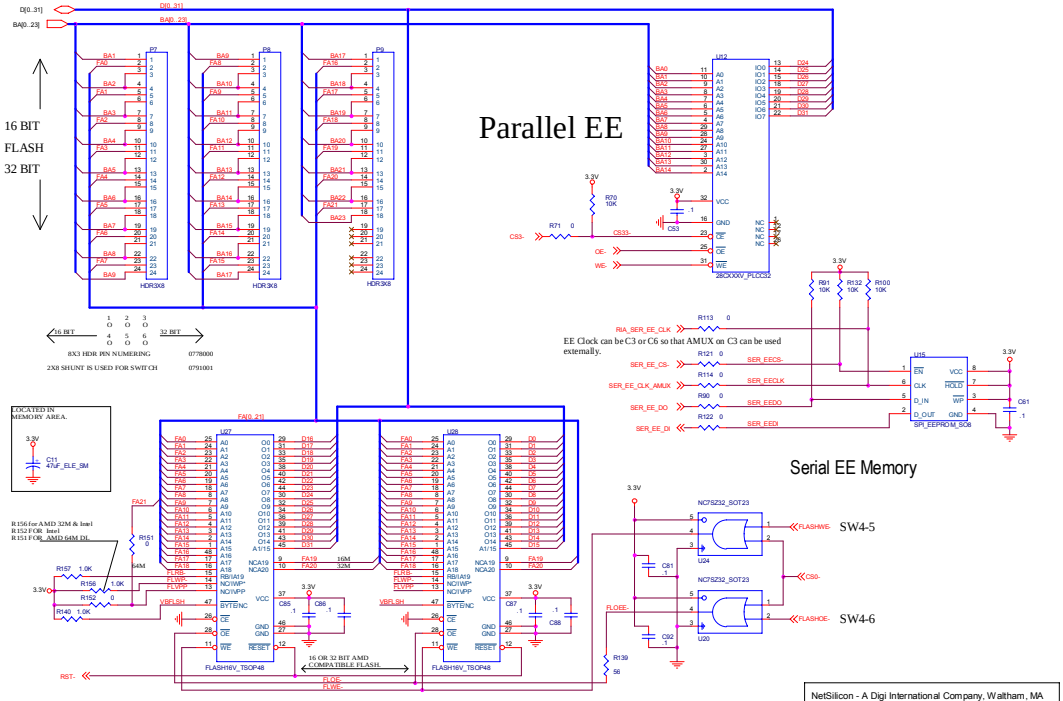
AMP #767054-1 Pin 44 = alignment hole; Pin 45-46 are for the optional latch securing holes.

NetSilicon - A Digi International Company, Waltham, MA

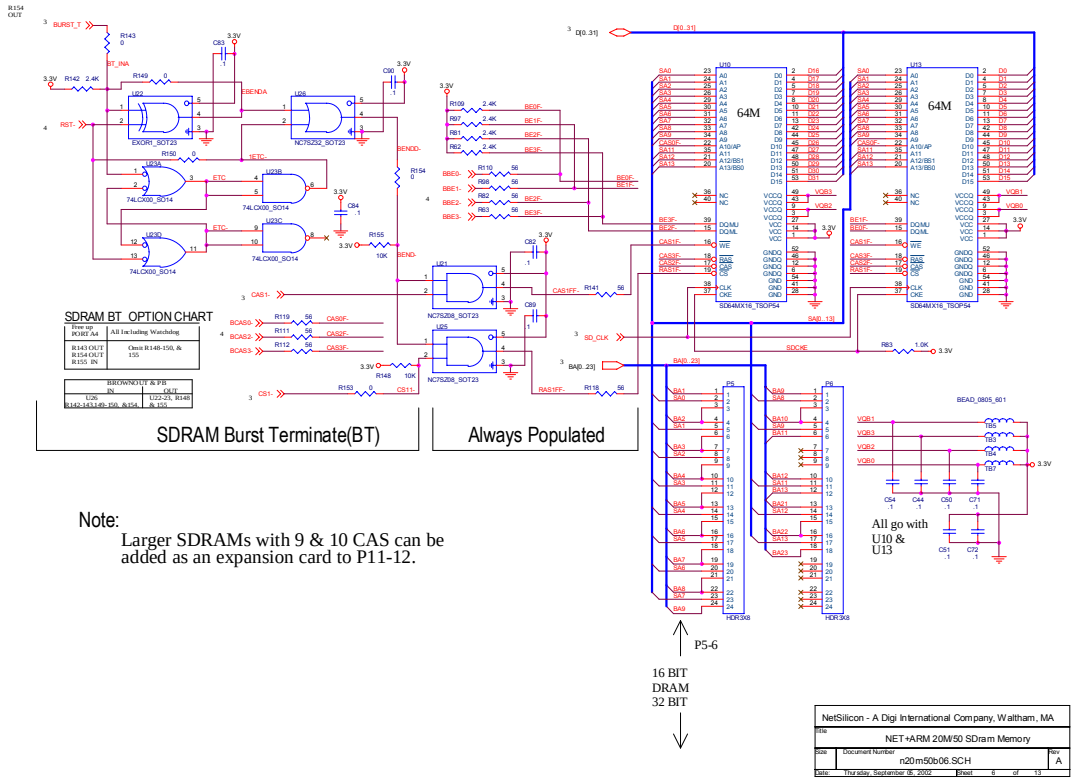
Title: NET+ARM 20M/50 Emulator Hdrs., Jtag, & Addr., Buffers

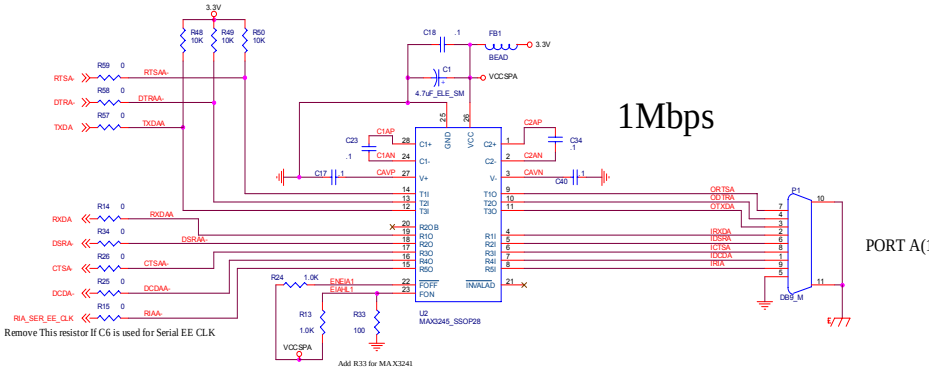
Size: | Document Number: n20m50b04.SCH | Rev: B

Date: Thursday, September 05, 2002 | Sheet 4 of 13

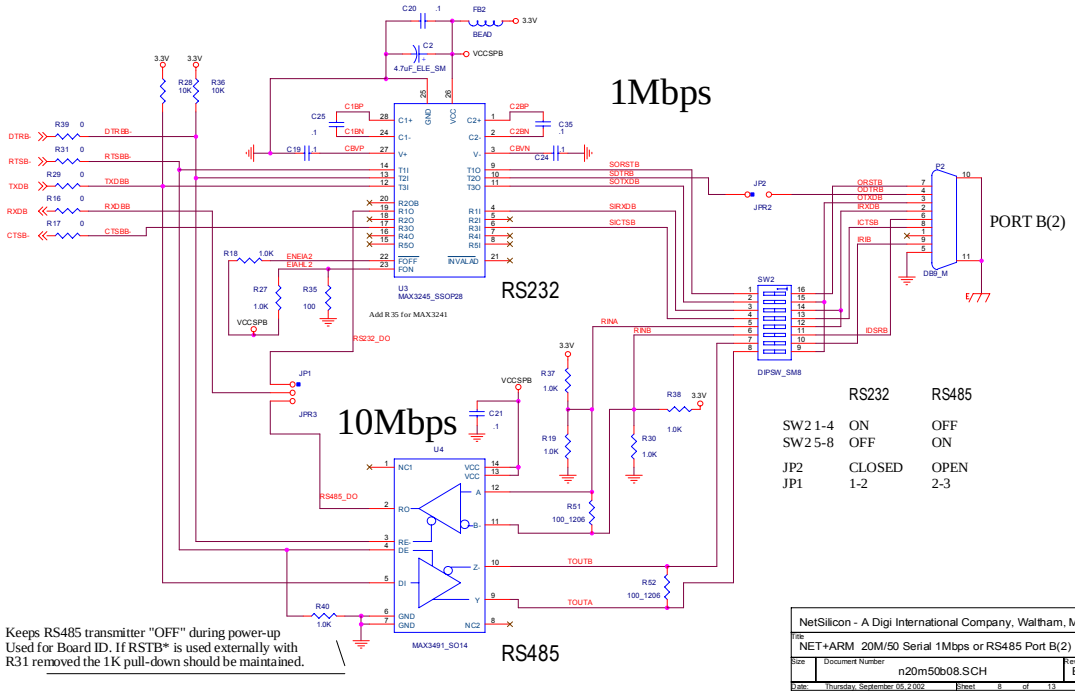


FLASH: x16 or x32

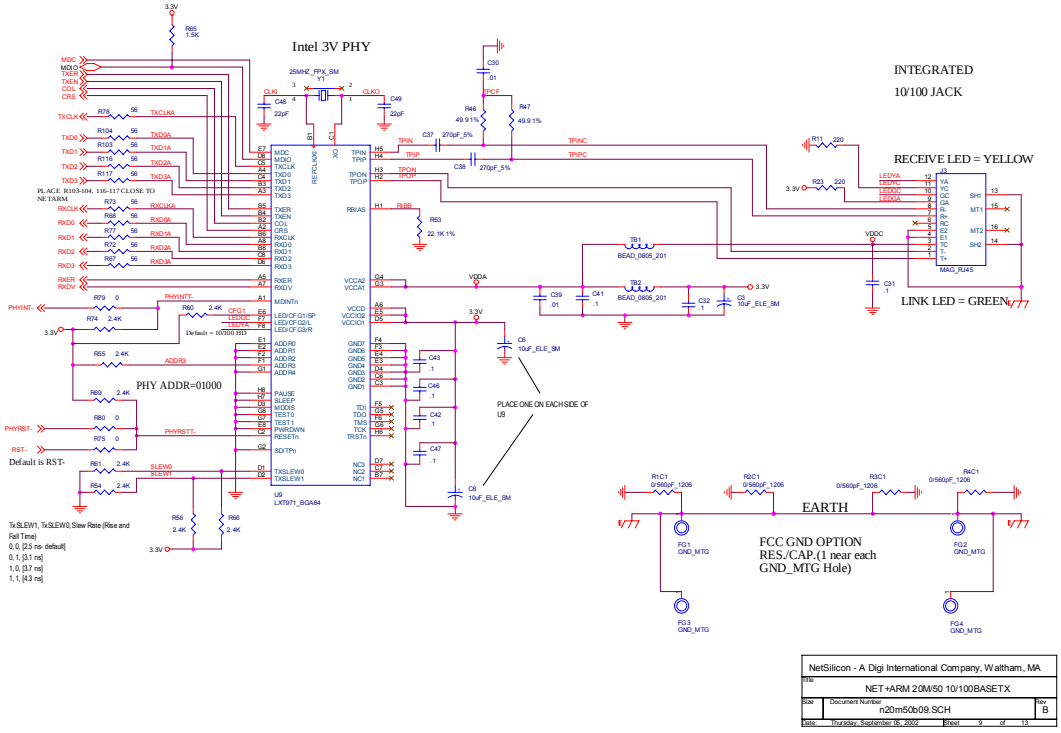

SDRAM BT OPTION CHART
Pow up PORT A4
All Including Watchdog
R143 OUT R154 OUT R155 IN
Omit R148-150, & 155
BROWNOUT & PB IN
OUT
U26
U22-23, R148 & 155
SDRAM Burst Terminate(BT)
Always Populated
Note:
Larger SDRAMs with 9 & 10 CAS can be added as an expansion card to P11-12.
P5-6
16 BIT DRAM 32 BIT
All go with U10 & U13
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM 20M/50 SDram Memory
n20m50b06.SCH
Thursday, September 26, 2002

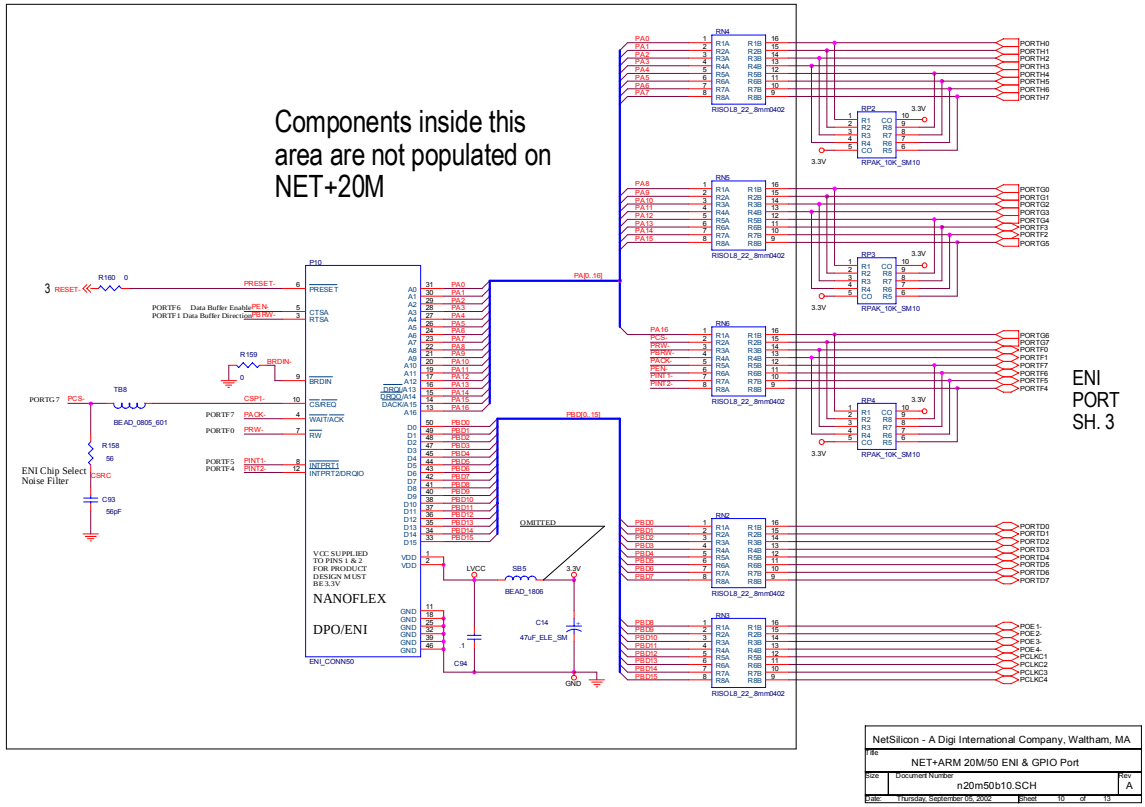


NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM 20M/50 Serial 1Mbps		
Size	Document Number: n20m50b07.SCH	Rev: A
Date: Thursday, September 05, 2002	Sheet 7 of 13	

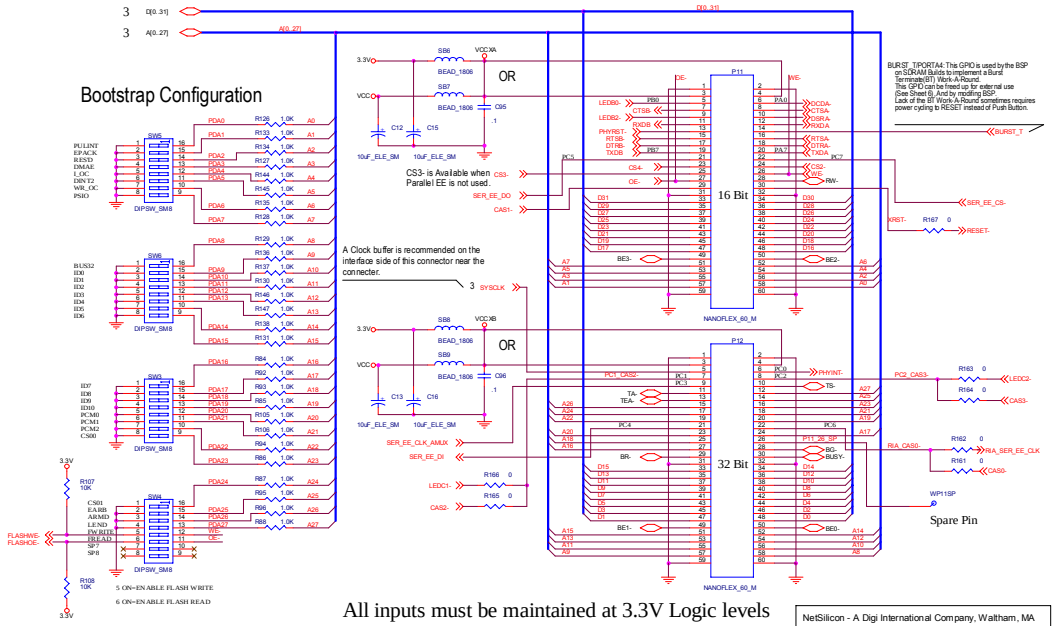


	RS232	RS485
SW2 1-4	ON	OFF
SW2 5-8	OFF	ON
JP2	CLOSED	OPEN
JP1	1-2	2-3


Intel 3V PHY
INTEGRATED
10/100 JACK
RECEIVE LED = YELLOW
LINK LED = GREEN
PHY ADDR=01000
Default is RST-
PLACE ONE ON EACH SIDE OF U8
EARTH
FCC GND OPTION
RES./CAP.(1 near each GND_MTG Hole)
PLACE R103-104, 116-117 CLOSE TO NETARM
TxSLEW1, TxSLEW0, Slew Rate (Rise and Fall Time)
0, 0, [2.5 ns- default]
0, 1, [3.1 ns]
1, 0, [3.7 ns]
1, 1, [4.3 ns]
U9
LXT971_BGA64
MAG_RJ45
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM 20M/50 10/100BASETX
n20m50b09.SCH
Thursday, September 05, 2002

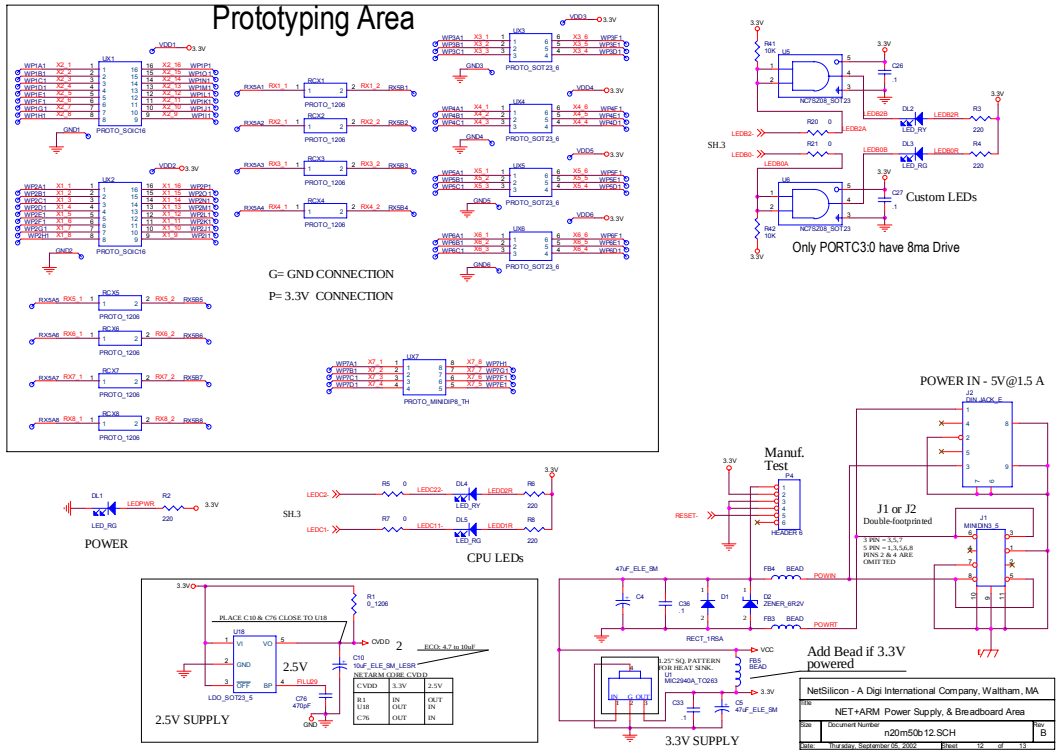

Components inside this area are not populated on NET+20M
ENI PORT SH. 3
ENI Chip Select Noise Filter
NANOFLEX
DPO/ENI
VCC SUPPLIED TO PINS 1 & 2 FOR PRODUCT DESIGN MUST BE 3.3V
OMITTED
ENI_CONN50
RISOL8_22_8mm0402
RPAK_10K_SM10
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM 20M/50 ENI & GPIO Port
n20m50b10.SCH
Thursday, September 05, 2002

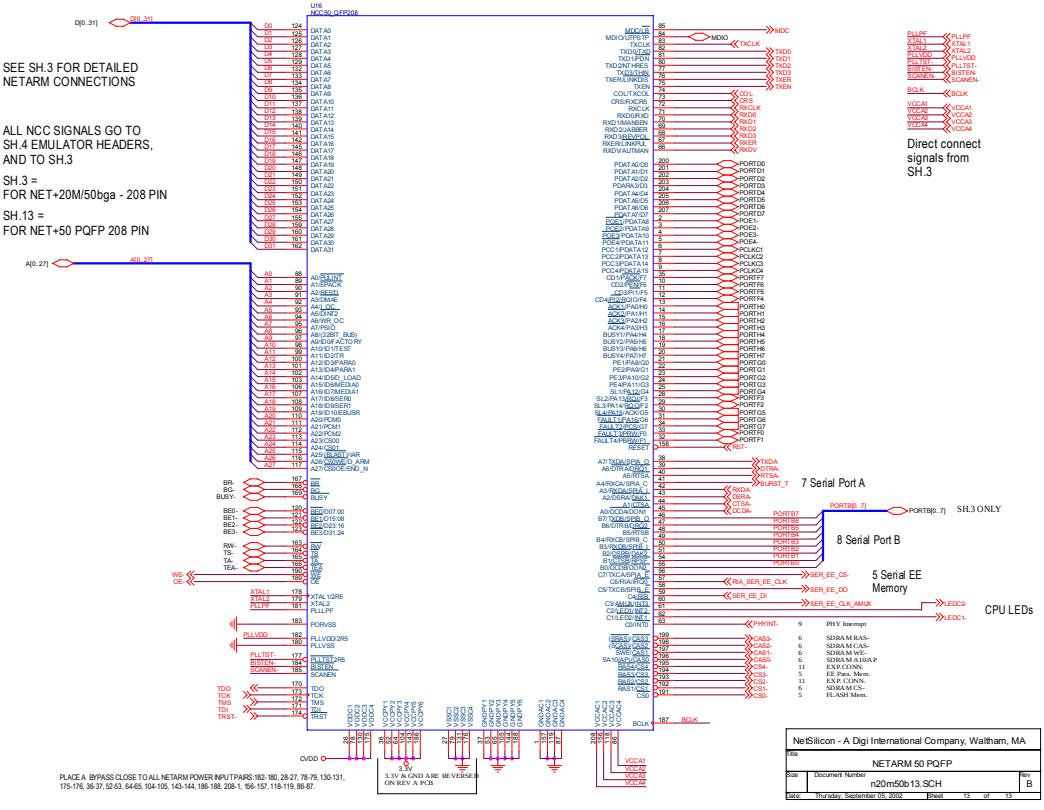
Expansion Connectors



All inputs must be maintained at 3.3V Logic levels

NetSilicon - A Digi International Company, Waltham, MA	
Title: NET+ARM 20M/50 Expansion & Dipswitches	
Size	Document Number: n20m50b11.SCH — Rev: A
Date: Thursday, September 05, 2002	Sheet 11 of 13


Prototyping Area
G= GND CONNECTION
P= 3.3V CONNECTION
Only PORTC3:0 have 8ma Drive
Custom LEDs
POWER IN - 5V@1.5 A
J1 or J2
Double-footprinted
Manuf.
Test
POWER
CPU LEDs
2.5V SUPPLY
3.3V SUPPLY
Add Bead if 3.3V
powered
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM Power Supply, & Breadboard Area
n20m50b12.SCH


SEE SH.3 FOR DETAILED NETARM CONNECTIONS
ALL NCC SIGNALS GO TO SH.4 EMULATOR HEADERS, AND TO SH.3
SH.3 = FOR NET+20M/50bga - 208 PIN
SH.13 = FOR NET+50 PQFP 208 PIN
Direct connect signals from SH.3
7 Serial Port A
8 Serial Port B
5 Serial EE Memory
CPU LEDs
SH.3 ONLY
PLACE A BYPASS CLOSE TO ALL NETARM POWER INPUT PAIRS 182-180, 28-27, 78-79, 130-131, 175-176, 36-37, 52-53, 64-65, 104-105, 143-144, 186-188, 208-1, 156-157, 118-119, 86-87.
3.3V & GND ARE REVERSED ON REV A PCB
NetSilicon - A Digi International Company, Waltham, MA
NETARM 50 PQFP
n20m50b13.SCH
Thursday, September 05, 2002

NET+Works Development Board Bill of Materials

CHAPTER 3

This chapter provides the bill of materials (BOM) for the NET+Works NET+50 development board.

BOM — NET+50 development board

This table provides information for each part in the PCBA NET+50 development board bill of materials (manufactured item 6151001):

- Part number (PN)
- Reference description (Ref desc)
- Description (Desc)
- Manufacturer (Mfg)
- Manufacturer part number (Mfg PN)

PN	Ref desc	Desc	Mfg	Mfg PN
0005907	U27, 28	FLASH ROM 512KX16 3.3V TSOP48	Fujitsu	MBM29LV800BA90PFTN
			ST Micro	M29W800AB90NS
			AMD	AM29LV800BB-90EC
0006950	U12	EEPROM 8K 3.3V PLCC32	Atmel	AT28LV64B-25J OR 20JC
			Catalyst	CAT28LV64N-3OTE13
0006961	U15	EEPROM MEMORY SPI 64K 8192X8	NetSilicon	0006961
			Atmel	AT25640-10PI-2.7
			Fairchild	FM25C640ULM8
			Integrated Silicon Solutions, Inc	IS25C64-3G
0041906	U10, 13	SDRAM 64M X 16 3.3V (tRFC 67.5ns or less) TSOP54	Micron	MT48LC4M16A2TG-75:G MT48LC4M16A2TG-7E:G MT48LC4M16A2P-75:G MT48LC4M16A2P-7E:G
			ISSI	IS42S16400B-7TL
			Elpida	EDS6416AHTA-75-E
			Etron Tech, Inc.	EM638165TS-7 EM638165TS-7G
			Samsung	K4S641632H-UC(L)75
0122938	U22	IC 2INPUT EX-OR SINGLE GATE	Toshiba	TC7SH86FTE85L
			Fairchild	NC7SZ86M5X

PN	Ref desc	Desc	Mfg	Mfg PN
0122939	U5-7, 19, 21, 25	IC 2 INPUT AND SINGLE GATE 3.	Toshiba	TC7SZ08FTE85L
			Fairchild	NC7SZ08M5X
0122940	U20, 24, 26	IC 2 INPUT OR SINGLE GATE 3.3	Toshiba	TC7SZ32FTE85L
			Fairchild	NC7SZ32M5X
0122951	U8	IC MAX811 VOLT MONITOR 4 PIN	Maxim	MAX811-SEUS-T
			Analog Devices	ADM811SART
0122957	U9	IC 10/100 PHY 3.3V 64 PIN PBG	NetSilicon	0122957
			Intel	LXT971ABC
0125908	U11, 14	IC 16-BIT TRANSCEIVER3.3V SS	Texas Instruments	SN74LVC16245ADLR
			Pericom	PI74LCX16245VX
			Integrated Device Tech.	74LVC16245APV
			Fairchild	74CX16245MEA
0125911	U23	IC 74LCX00 QUAD 2INPUT NAND G	Texas Instruments	SN74LVC00ADR
			Toshiba	74LCX00FN
			Fairchild	74LCX00M
			ST Micro	74LCX00M
0125925	U2, 3	IC TRANSCEIVER 3.3V 1MBPS 28	Maxim	MAX3245CAI
0125926	U4	IC TRANSCEIVER 3.3V 12MBPS RS	Maxim	MAX3491ECSD
0133995	U18	REGULATOR 2.5V SOT23-5 150MA	Maxim	MAX8877EUK25-T
			IMP	IMP2185-2.5JUK/T
			MICREL	MIC5207-2.5BM5
			Telcom	TC1015-2.5VCT713
0133020	U17	REGULATOR LDO 1.25A 3.3V TO26	National Semi Conductor	LM3940IS-3.3
			MICREL	M1C2904A33BU
0137003	U17	IC NET+50 BGA (ATMEL)	NetSilicon	0137003
0143900	D1	DIODE 1.5A RECTIFIER SOD-87	Phillips	BYD17D

PN	Ref desc	Desc	Mfg	Mfg PN
0144900	D2	DIODE ZM4735A ZENER ZM-41(SM)	Diodes Inc	ZM4735A-13
			American Power Device	ZM4735A-13
			ITT	ZM4735A-13
0163110	SW2-6	SWITCH SPST 8 POS SM DIP 16PI	C & K	TD08H0SK1
0167000	SW1	SWITCH PUSH BUTTON	C & K	PTS635SL50
0175902	Y3	CRYSTAL 18.432 MHZ 20 PF (SMT	Epson	MA40618.432M-GO
			Fox	FPX-18.432-20
			HEC	HEC3A-18.432-MHZ-20PF
0175903	Y1	CRYSTAL 25 MHZ FUNDAMENTAL 20	Epson	MA40625.000M-GO
			Fox	FPX-SM-25
			HEC	HEC-3A-25MHZ-20PF500PPM
0186000		FOOT NETSPRINT CABINET BASE	Green Rubber	0186000
0190900	FB1-4	FERRITE BEAD 9OZ @ 100MHZ (SM	ACT	FB863226-Y7
			FAIR-RITE	2743021447
0190902	TB1, 2, 6	FERRITE BEAD 20OZ 100MHZ (SM	TDK	ACB2012M-150T
			Murata	BLM21B201S
			Steward	LI0805H151R-00
			Steward	LI0805D121R
0190903	TB3-5, 7, 8	FERRITE BEAD 75OZ 100MHZ (SM	Murata	BLM21B601S-PT or B102S-PT
			ACT	LCB-0805-TR
			FAIR-RITE	2508058017Z0
0190950	SB1-4, 6, 8	EMI FILTER FERRITE CHIP EIA	Murata	BLM41A800SPT
			Associated Comp. Tech	DCB-1806-3.5A
0261920	C37, 38	CAP 270 PF 50V 5% NPO SM0603	NetSilicon	0261920
			Murata	GRM1885C1H271JA01E
			AVX	06035C0G271JAT2A

PN	Ref desc	Desc	Mfg	Mfg PN
0263901	C48, 49, 62, 68	CAP 22 PF 50V 5% 0603	Vitramon	VJ0603A2220JXAAT
			NIC	NMC0603NPO220J50TR
			KEMET	C0603C220J5GAC
			AVX	06035A220JAT2A
0265901	C76	CAP 470 PF 50V 10% 0603	NetSilicon	0265901
			NIC	NMC0603X7R471J50TRP
0268902	C29	CAP .001 MFD 50V 10% 0603	Vitramon	VJ0603Y102KXAAT
			AVX	06035C102KAT2A
0270901	C30, 39	CAP .01 MFD 50V 10% 0603	Vitramon	VJ0603Y103KXAAT
			KEMET	C0603C103K5RAC
			AVX	06035C103KAT2A
0272903	C17-27, 28, 31-36, 40-47, 50-61, 63, 64, 66, 69-75, 77, 79-92, 94, 95, 96	CAP .1 MFD 16V 10% 0603	Vitramon	VJ0603Y104KXJAT
			NIC	NMC0603X7R104K16TR
			AVX	0603YC104KAT2A
0280951	C3, 6, 8, 12, 13, 15, 16	CAP 10UF 16V ELE SM B SIZE	NIC	NACE100M16V4X5.5TR13
			Panasonic	ECEV1CA100R
			Nichicon	UWX1C100MCR1GB
			CAL Chip	GACE100M16V4X5.5TR13
0282005	C65	CAPACITOR .0015uF 16V, 10%, 0603	KEMET	C0603C152K5RAC
			AVX	06035C152KAT2A
0285014	C10	CAP 10uF 16V 20% ELE LOW ESR		
0288002	C1, 2, 7, 9	CAP 4.7 MF 25V 20% SIZE B ELE	Panasonic	ECEV1EA4R7SR
			Panasonic	ECEV1VA4R7SR
			CAL Chip	GACE4R7M25V4X5.4TR13

PN	Ref desc	Desc	Mfg	Mfg PN
0288902	C4, 5, 11, 14	CAP 47 MF 16v 20% SIZE D ELE	NIC	NACE470M16V6.3X5.5TR13
			Panasonic	ECEV1CA470ER
			CAL Chip	GACE470M16V6.3x5.5 TR13
0288905	C78	CAP .015UF X7R 5V MIN 0603	NetSilicon	0288905
			Murata	GRM188F51E153ZA01D
			Panasonic	ECJ-1VB1C153K
			Panasonic	ECJ-1VF1H153Z
0370900	R1C1, R2C1, R3C1, R4C1	RES 0 OHM 1/8W 5% (SM 1206)	Any	0370900 any MFG
0370902	R5, 7, 9, 14-17, 20, 21, 25, 26, 29, 31, 34, 39, 45, 57-59, 71, 75, 79, 90, 114, 121, 122, 143, 152-154, 159, 160, 162, 163, 166, 167	RES 0 OHM 5% 0603	NetSilicon	0370902
			Panasonic	ERJ3GEY0R00V
0371902	R63, 67, 68, 72, 73, 77, 78, 82, 98, 103, 104, 110-112, 116-119, 139, 141	RES 56 OHM 5% 1/16w 0603	NetSilicon	0371902
			Panasonic	ERJ3GEYJ560V
0377900	R51	RES 100 OHM 1/8W 1% (SM 1206)	NetSIlicon	0377900
			Tad Components, Inc.	CR181000FM
0377902	R64, 99	RES 100 0HM 5% 1/16W 0603	NetSilicon	0377902
			Panasonic	ERJ3GEYJ101V

PN	Ref desc	Desc	Mfg	Mfg PN
0377904	R123	RES 820 OHM 5% 1/16W 0603	NetSilicon	0377904
			AVX	CR10-821J-T
			Panasonic	ERJ3GEYJ821V
0384901	R2-4, 6, 8, 11, 23	RES 220 OHM 5% 1/16W 0603	NetSilicon	0384901
			AVX	CR10-221J-T
			Panasonic	ERJ3GEYJ221V
0400003	RN1-6, 2-6	RES ARRAY (8 RESISTOR) 22 OHM	NetSilicon	0400003
			KOA	CN1J8TE220J
			CTS Corporation	742C163
0400020	RP2-4	RES NET 10K OHM 1/16W 5%	NetSilicon	0400020
0400021	RP1	RES NET 1K OHM 1/16W 5%	NetSilicon	0400021
0400028	R65	RES 1.5K 5% 1/16W 0603	NetSilicon	0400028
			AVX	CR10-152J-T
			Panasonic	ERJ3GEYJ152V
0400904	R13, 18, 22, 24, 27, 30, 37, 40, 83-88, 92-96, 105, 106, 126-131, 133-138, 140, 144-147, 156, 157	RES 1K 5% 1/16W 0603	NetSilicon	0400904
			AVX	CR10-102J-T
			Panasonic	ERJ3GEYJ102V
0416906	R46, 47	RES 49.9 OHM 1/16W 1% 0603	NetSilicon	0416906
			AVX	CR10-49R9F-T
0424904	R10, 12, 28, 36, 41-43, 48-50, 70, 89, 91, 100, 107, 108, 132	RES 10K 5% 1/16W 0603	NetSilicon	0424904

PN	Ref desc	Desc	Mfg	Mfg PN
			AVX	CR10-103J-T
			Panasonic	ERJ3GEYJ103V
0425902	R124	RES 15 OHM 5% 1/16W 0603	NetSilicon	0425902
			AVX	CR10-242J-T
			Panasonic	ERJ3GEYJ242V
0432902	R54, 55, 60-62, 69, 74, 76, 81, 97, 109, 120, 142	RES 2.4K 5% 1/16W 0603	NetSilicon	0432902
			AVX	CR10-242J-T
			Panasonic	ERJ3GEYJ242V
0511930	R53	RES 22.1K 1% 1/16W 0603	NetSilicon	0511930
			AVX	CR10-221F-T
0606000	DL1,3,5	LED GREEN (1) PCB MOUNT RIGHT	Kingbrite	L-73CB/1GDA-24
			P-TEK	PL506-1GRA
			LITE ON	LTL-53311
0607000	DL2,4	LED YELLOW (1) PCB MOUNT RIGH	Kingbrite	L-73CB/YDA24
			P-TEK	PL506-1Y.112
			LITE ON	LT553-11
0700010	J3	CONN PULSE THRU HOLE TAB DN R	Pulse	J0026D21B
0705000	J2	CONN DIN JACK 5 CONTACT 180 D	Singatron	DJ-021-5P
0752101	P1, 2	CONN 9 PIN RA MALE .318FP (DB	NetSilicon	0752101
			KYCON	K22-E9P-N
0773010	J4-8	CONN VERTICAL 38 POS MICTOR	NetSilicon	0773010
			AMP	767054-1
0777550	P10	HEADER 50 PIN BOX 4 ROW STAGG	MOUSER	554-50NFHL12GT
			Circuit Assembly Corp	CA-50NFHL-12GT

PN	Ref desc	Desc	Mfg	Mfg PN
0777551	P11, 12	HEADER 60 PIN BOX 4 ROW STAGG	Circuit Assembly Corp	CA-60NFHL-12GT
0778000	P5-9	HEADER 3X8 TERMINAL STRIP (ST	Singatron	2203-24-S-02
0790001	JP1	HEADER 3PIN SINGLE ROW STRAIG	Singatron	201-1X3-GS
			RDI	PHSS03G1
0790002	JP2	HEADER 2PIN SINGLE ROW STRAIG	Singatron	2201-2-S-02
			RDI	PHSS02G1
0790004	P4	HEADER 6PIN SINGLE ROW STRAIG	Singatron	2201-6-S-02
			RDI	PHSS06G1
0790012	P3	HEADER 7 X 2 DOUBLE ROW STRAI	Singatron	2202-14-S-02
			RDI	PHDS14G1
0791000	JP1, 2	JUMPER MINI 2-POSITION .1"SPA	NetSilicon	0791000
			Eastern Micro Devise	146-02
			Eastern Micro Devise	206-B1
			Berg	6547-004
			Berg	6547-005
			Project Resources	0500-B-G-02-6-1
0791001	P5-9	SHUNT (JUMPER) 2X8 .1"SPACING	FAI Tech	MJX-MD-8
			FRAMATOME CONN	69145-216
			COM CON Connectors	CCM1J235-08G
1077000	ASM to J2	SCREW 2-56 MACH 1/4"L SLOT RD	NetSilicon	1077000
1951000		PWB DEVICE SERVER BGA	NetSilicon	1951000
DWG6151XXX		ASSY DWG DEVICE SERVER BGA	NetSilicon	DWG6151XXX

PN	Ref desc	Desc	Mfg	Mfg PN
SCH1951000		SCHEMATIC DEVICE SERVER BGA	NetSilicon	SCH1951000
XXXNONPOP	C67, 93; FB5; J1; R1, 19, 32, 33, 35, 38, 44, 52, 55, 56, 66, 80, 101, 102, 113, 115, 125, 148-151, 155, 158,161, 164, 165; SB5, 7, 9; U16; Y2	COMPONENTS NOT POPULATED	NetSilicon	XXXNONPOP

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