SECTION NINE

Programming Information

Programmers and developers writing new software for the SYNC/570 or SYNC/570i need the programming information presented in this section. Refer to the Hitachi HD64570 documentation for additional information. Programming diagnostics are available in a Developer's Kit.

Information in this section regarding two-port boards applies to both SYNC/570 and SYNC/570i. Information regarding four-port boards applies to the four-port SYNC/570i. The information relevant to both ISA and Micro Channel buses follows the bus specific information.

ISA Bus Interface

The ISA version of the SYNC/570 or SYNC/570i requires 16 bytes of I/O space (in the 0x000 -0x3ff range) and 16KB of memory space (in the 0x000 - 0xffffff range). A 16 bit data path provides access to the memory.

I/O Select Switch

The starting address of the adapter's I/O space is determined by a switch. Refer to Section 5 for switch setting information. Each switch (segment) on the switch block corresponds to the ISA address bus as follows.

ISA Address	Switch Block Segment
A4	1
A5	2
A6	3
A7	4
A8	5
A9	6

Located in the I/O space are registers which control the memory and the SCA. The driver supporting the adapter is responsible for programming these registers during initialization. These registers are located at an offset from the starting I/O address. Refer to "I/O Registers" for a summary of this offset register set.

Interrupt Select Register

The Interrupt Select Register (*Read/Write*) is located in a byte within I/O space at an offset of 0xC from the adapter I/O base address. It provides the card enable, IRQ select, and two bits of the starting memory address in the format shown below.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
not used	not used	CMA15	CMA14	ISEL2	ISEL1	ISEL0	CEN
X	X	memory value		interrupt value			0=disable 1=enable

Bit 0 represents the Card Enable bit. A 1 in this position enables the IRQ and memory of the adapter, and is recommended for use at initialization. Use MEM of offset 0x8 to turn the board memory on and off. The memory address register (at an offset of 0xD from the adapter base address) should be set prior to setting this bit to 1.

Bits 1, 2, and 3 select the interrupt as shown below.

ISEL2	ISEL1	ISEL0	Interrupt
0	0	0	disabled
0	0	1	IRQ 3
0	1	0	IRQ 5
0	1	1	IRQ 7
1	0	0	IRQ 10
1	0	1	IRQ 11
1	1	0	IRQ 12
1	1	1	IRQ 15

Bits 4 and 5 in conjunction with the Memory Address Register select the starting memory address.

Memory Address Register

The Memory Address Register (*Read/Write*) is located in a byte within I/O space at an offset of 0xD from the adapter I/O base address. It provides the starting memory address of the adapter (along with the CMA14 and CMA15 bits of the Interrupt Select Register). Bits 0 through 7 contain the values for CMA (Compare Memory Address) 16 through 23 respectively.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CMA23	CMA22	CMA21	CMA20	CMA19	CMA18	CMA17	CMA16

Configurations for several common memory addresses are shown below.

Address	CMA23	CMA22	CMA21	CMA20	CMA19	CMA18	CMA17	CMA16	CMA15	CMA14
D0000H	0	0	0	0	1	1	0	1	0	0
D4000H	0	0	0	0	1	1	0	1	0	1
D8000H	0	0	0	0	1	1	0	1	1	0
DC000H	0	0	0	0	1	1	0	1	1	1

Micro Channel Bus Interface

The Micro Channel version of the SYNC/570 or SYNC/570i requires 16 bytes of I/O space (in the 0x000 -0xfff range) and 16KB of memory space (in the 0x000 - 0xffffff range). A 16 bit data path provides access to the memory.

A Micro Channel Programmable Option Select (POS) ID of 0x6163 identifies the adapter. Three POS registers set the memory and I/O addresses and the IRQ of the adapter. (Refer to Section 6 for adapter configuration using the ADF file.) Operating systems have the ability to read (adapter memory, I/O and IRQ requirements) or modify these registers. The POS registers, summarized below, are written after a power on reset.

Address	Read	Write
0x100	ID Code = 0x63	
0x101	ID Code = 0x61	
0x102	Interrupt Select	Interrupt Select
0x103	IO Address Select	IO Address Select
0x104	Memory Address Select	Memory Address Select

The paragraphs below and following summarize the register set by address.

0x100

The POS register at this address provides a two byte POS identification code and always reads 0x63.

0x101

The POS register at this address provides a two byte POS identification code and always reads 0x61.

0x102

The POS register at this address provides the card enable, IRQ select, and two bits of the starting memory address in the format shown below.

Bit 0 represents the Card Enable bit. A zero in this position disables all functions of the adapter (memory space, I/O space, and interrupts.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
not used	not used	CMA15	CMA14	ISEL2	ISEL1	ISEL0	CEN
X	X	memory value		interrupt value			0=disable 1=enable

Bits 1, 2, and 3 select the interrupt as shown below.

ISEL2	ISEL1	ISEL0	Interrupt
0	0	0	disabled
0	0	1	IRQ 3
0	1	0	IRQ 5
0	1	1	IRQ 7
1	0	0	IRQ 10
1	0	1	IRQ 11
1	1	0	IRQ 12
1	1	1	IRQ 15

Bits 4 and 5 in conjunction with the POS register at 0x104 select the memory address. More information regarding memory selection is given on the following page.

0x103

The POS register at this address provides the starting I/O address of the adapter and is structured as shown below.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CIA11	CIA10	CIA9	CIA8	CIA7	CIA6	CIA5	CIA4

The 16 bytes of I/O space can be located 0x0 - 0xfff at any 16 byte boundary. Each CIA is compared to the respective address line of the Micro Channel bus. A15 - A12 are always compared to 0.

Configurations for several common I/O base addresses are shown below.

Address	CIA11	CIA10	CIA9	CIA8	CIA7	CIA6	CIA5	CIA4
300H	0	0	1	1	0	0	0	0
730H	0	1	1	1	0	0	1	1
330H	0	0	1	1	0	0	1	1

Located in the I/O space are registers which control the memory and the SCA. The driver supporting the adapter is responsible for programming these registers during initialization. These registers are located at an offset from the starting I/O address and are **not** POS registers. Refer to "I/O Registers" for a summary of this offset register set.

0x104

The POS register at this address provides the starting memory address of the adapter. Bits 0 through 7 contain the values for CMA (Compare Memory Address) 16 through 23 respectively. (CMA14 and CMA15 are bits 4 and 5 of address 0x102.) Each CMA is compared to the respective address line of the Micro Channel bus. This allows the full 16MB addressing range (0x000 - 0xffffff) to be supported in 16KB increments. The structure for this register is shown below.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CMA23	CMA22	CMA21	CMA20	CMA19	CMA18	CMA17	CMA16

Configurations for several common memory addresses are shown below.

Address	CMA23	CMA22	CMA21	CMA20	CMA19	CMA18	CMA17	CMA16	CMA15	CMA14
D0000H	0	0	0	0	1	1	0	1	0	0
D4000H	0	0	0	0	1	1	0	1	0	1
D8000H	0	0	0	0	1	1	0	1	1	0
DC000H	0	0	0	0	1	1	0	1	1	1

Information Relevant to Both ISA and Micro Channel Buses

Unless otherwise noted, the remaining paragraphs in this programming section provide information which is common to both ISA and Micro Channel versions of the SYNC/570 and SYNC/570i.

I/O Registers

The I/O registers are located at an offset from the starting I/O address. A summary of this register set is shown below.

Address	Read	Write
Base Address + 0x0	Reserved	
Base Address + 0x1	Reserved	
Base Address + 0x2	Reserved	
Base Address + 0x3	Bus, Memory and Interface Type	
Base Address + 0x4	Adapter Revision	
Base Address + 0x5	Port Number	
Base Address + 0x6	Supported Handshake	
Base Address + 0x7	DCD and Interrupt Status	
Base Address + 0x8		Memory and SCA Enable
Base Address + 0x9		Transmit Clock and DTR Control 0 & 1
Base Address + 0xA	Security PAL	Security PAL
Base Address + 0xB	Interrupt Acknowledge 0 & 1	
Base Address + 0xC	*ISA Only - Interrupt Select*	*(refer to Page 22)*
Base Address + 0xD	*ISA Only - Memory Select*	*(refer to Page 23)*
Base Address + 0xE	Interrupt Acknowledge 2 & 3	Transmit Clock and DTR Control 2 & 3
Base Address + 0xF		

Unused registers are reserved for future use.

Bus, Memory, and Communications Interface Register

The PC bus type, memory configuration, and communications interface type for the adapter are located in a byte within I/O space at an offset of 0x3 from the adapter I/O base address. This *Read Only* register is formatted as follows.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IT2	IT1	IT0	MS2	MS1	MS0	BUS1	BUS0
communications interface type value			memory configuration value			bus type value	

Bits 0 and 1 define the PC bus type for the adapter as follows:

Bus Type	BUS1	BUS0
ISA	0	0
Micro Channel	0	1
EISA	1	0

Bits 2, 3, and 4 define the amount of on-board memory. This memory is not field upgradeable.

Memory Size	MS2	MS1	MS0
64KB	0	0	0
128KB	0	0	1
256KB	0	1	0
512KB	0	1	1

Bits 5, 6, and 7 define the specific communications interface type for the adapter.

Communication Type	IT2	IT1	IT0	
EIA-232	0	0	0	(SYNC/570)
V.35/EIA-232	0	0	1	(SYNC/570i)
EIA-530	0	1	0	(SYNC/570i)
X.21	0	1	1	(SYNC/570i)
Combination	1	1	0	(SYNC/570i)

(Combination communication: Port 1 = EIA 530, Port 2 = X.21)

V.35 Specific The V.35 daughterboard has jumpers to change from a V.35 interface to an EIA-232 interface (refer to Appendix B). Regardless of the jumper position, IT2-IT0 will always contain 001 to define the V.35 daughterboard.

X.21 Specific The X.21 daughterboard supports three types of cables. One cable supports the X.21 interface. Another cable supports the EIA-530 standard. The third cable is a combination cable, allowing a X.21 interface on one port and a EIA-530 interface on the second port.

When the X.21 cable is installed, IT2-IT0 will contain 011. When the EIA-530 cable is installed, IT2-IT0 will contain 010. When the combination cable is installed, IT2-IT0 will contain 110.

Adapter Revision Register

A revision number is located in a byte within I/O space at an offset of 0x4 from the adapter I/O base address. Bits 0 through 3 (Rev0-Rev3) of this *Read Only* register indicate the feature set revision level of the adapter. This level will be updated in the event a new feature is added or changes made which will affect programming. This is not the assembly revision of the adapter.

Port Number Register

The number of communication ports on the adapter are located in a byte within I/O space at an offset of 0x5 from the adapter I/O base address. (A two port board will have a 0x2 at this location.) This is a *Read Only* register.

Supported Handshake Register

The Specific handshake signals supported by each port on the adapter is located in a byte within I/O space at an offset of 0x6 from the adapter I/O base address. This Read Only register defines only the support for handshake signals and **does not represent the current status of signals themselves**. This is important for versions of the adapter that may have

differing connector types that support limited numbers of pins for handshake signals.

The structure of the register is shown below.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DCD	RI	DSR	CTS	not used	not used	RTS	DTR

A bit value of 0 indicates that the signal is unavailable.
A bit value of 1 indicates that the signal is available.

X.21 Specific The Indicator and Control Signals on the X.21 daughter board correspond to DSR and DTR respectively.

DCD and Interrupt Status Register

The interrupt status and DCD support for the adapter are located in a byte within I/O space at an offset of 0x7 from the adapter I/O base address. This *Read Only* register is structured as follows.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
not used	INT1	INT0	DCD3	DCD2	DCD1	DCD0	Board Level Interrupt
X	0=none 1=pending	0=none 1=pending	Port 3 0=active 1=inactive	Port 2 0=active 1=inactive	Port 1 0=active 1=inactive	Port 0 0=active 1=inactive	0=none 1=pending

The Hitachi HD64570 does not directly support DSR. DCD is supported directly with the HD64570, and the SYNC/570 or SYNC/570i connects this input to DSR in order to provide an interrupt on a change to DSR. Therefore, any reference to DCD in the user's manual for the Hitachi HD64570 will translate to DSR on the SYNC/570 or SYNC/570i. DCD is then provided in this register for compatibility with devices which support DCD.

The interrupt status for the adapter is defined with the Board Level Interrupt bit of this register. This is the logical "OR" of INT0 and INT1. When set to 0, there are no pending interrupts. INT0 indicates the interrupt status of ports 0 and 1. When set to 0, there are no interrupts pending. INT1 indicates the interrupt status of ports 2 and 3. When set to 0, there are no interrupts pending.

Memory and SCA Enable Register

The ability to enable the memory, set the window address, and enable the SCA of the adapter are located in a byte within I/O space at an offset of 0x8 from the adapter I/O base address. This Write Only register is structured as follows:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MEM	En_SCA	Sel_SCA	WIN4	WIN3	WIN2	WIN1	WIN0
0=disabled 1=enabled	0=disabled 1=enabled	0=SCA0 1=SCA1	Reserved for future use	Refer to the table on the following page			

Memory can be enabled or disabled via bit 7, the MEM bit, to allow multiple cards to reside at the same memory address. (0=disables; 1=enables.) This also disables the Hitachi HD64570 if it is enabled with En-SCA. This feature is best used on the ISA bus. The Micro Channel configurations program will mark all boards at the same memory address with conflicts.

When the Hitachi HD64570 is enabled via the En_SCA bit, one of the two devices will appear in the lower 256 bytes of each memory window (0=disables; 1=enables).

The Sel_SCA bit determines which SCA is enabled (0=SCA0; 1=SCA1). When En_SCA is set, a 0 in Sel_SCA selects the SCA controlling ports 0 and 1. When En_SCA is set, a 1 in Sel_SCA selects the SCA controlling ports 2 and 3. Access to the lower 256 bytes of memory of each window is possible only if En_SCA is cleared. A device may be enabled at all times if loss of 256 bytes/window is acceptable for the application.

The Hitachi HD64570 registers are located at the starting memory address, and all 256 registers of the chip are accessible.

The complete range of memory can be accessed through 16KB windows defined by the bits WIN0-WIN3. (WIN4 is reserved for future expansion and should always be set to 0.) The 16KB windows are accessed by the following bit combinations of WIN0-WIN3:

Address Relative to HD64570	WIN3	WIN2	WIN1	WIN0
0 - 3FFFH	0	0	0	0
4000 - 7FFFH	0	0	0	1
8000 - BFFFH	0	0	1	0
C000 - FFFFH	0	0	1	1
10000 - 13FFFH	0	1	0	0
14000 - 17FFFH	0	1	0	1
18000 - 1BFFFH	0	1	1	0
1C000 - 1FFFFH	0	1	1	1
20000 - 23FFFH	1	0	0	0
24000 - 27FFFH	1	0	0	1
28000 - 2BFFFH	1	0	1	0
2C000 - 2FFFFH	1	0	1	1
30000 - 33FFFH	1	1	0	0
34000 - 37FFFH	1	1	0	1
38000 - 3BFFFH	1	1	1	0
3C000 - 3FFFFH	1	1	1	1

Transmit Clock and DTR Control Register

The ability to support DTR and control the Transmit Clock signal for Ports 0 and 1 is located in a byte within I/O space at an offset of 0x9 from the adapter I/O base address. All bits are cleared with a power on reset. This *Write Only* register is structured as shown on the following page.

The RES bit of the register allows both SCAs to be reset. To reset the Hitachi HD64570, set RES bit to zero, wait at least 1000 nsec, and then set the RES bit to 1.

The TXCS1 and TXCS0 bits are used to select the desired mode of the bi-directional transmit clock for Ports 1 and 0 respectively. To use the transmit clock as an output, set this bit to 0. To use the transmit clock as an input, program the internal registers of the Hitachi HD64570 to make transmit clock an input prior to setting this bit.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
not used	RES	TXCS1	TXCS0	DTR1	DTR0	TX1	TX0
X	0=reset held 1=out of reset	Port 1 0=output 1=input	Port 0 0=output 1=input	Port 1 0=inactive 1=active	Port 0 0=inactive 1=active	Port 1 0=disable 1=enable	Port 0 0=disable 1=enable

WARNING

If this bit is set to 1 and the Hitachi HD64570 is still outputting the transmit clock, two outputs will be tied together and damage to the HD64570 is possible.

X.21 Specific

Only one clock can be active on the X.21 connector. When using the DCE clock source, the X.21 Signal Element Timing input drives the HD64570 receive clock directly. The HD64570 RXS register should specify "Receive clock source is RXC line input." The HD64570 TXS register should specify "Transmit clock source is Receive clock."

When using the DTE clock source, the X.21 DTE Signal Element Timing output is also used as the transmit and receive clocks. The HD64570 RXS register should specify "Receive clock source is Internal BRG output." The HD64570 TXS register should specify "Transmit clock source is Internal BRG output."

In both cases of X.21 clock sources, the SYNC/570 Transmit Clock and DTR Control register should specify the transmit clock as an output (TXCSn=0).

The Hitachi HD64570 does not directly support DTR. DTR is provided in this latch for compatibility with devices which require this signal.

Bits TX0 and TX1 of this register enable the transmitter of Ports 0 and 1 respectively. When set to 0 (transmitter disabled), data may be transmitted from the Hitachi HD64570, but the data will not appear at the external connector.

Security PAL Register

Refer to the *Digi Engineering Specification for the SYNC/570 Security PAL* for complete programming details. This PAL is the same for both the SYNC/570 and /570i.

Interrupt Acknowledge Register

The Interrupt Acknowledge Register for ports 0 and 1 is located in a byte within I/O space at an offset of 0xB from the adapter I/O base address. This register is *Read Only* and will return the value of IVR or IMVR of the Hitachi HD64570, depending on the state of VOS. This is used with the single acknowledge mode of the Hitachi HD64570.

WARNING

Reading this register with no interrupts pending will lock the system. Read the DCD and Interrupt Status Register for status.

Interrupt Acknowledge Register

The Interrupt Acknowledge Register for ports 2 and 3 is located in a byte within I/O space at an offset of 0xE from the adapter I/O base address. This register is *Read Only* and will return the value of IVR or IMVR of the Hitachi HD64570, depending on the state of VOS. This is used with the single acknowledge mode of the Hitachi HD64570.

WARNING

Reading this register with no interrupts pending will lock the system. Read the DCD and Interrupt Status Register for status.

Transmit Clock and DTR Control Register

The ability to support DTR and control the Transmit Clock signal for ports 2 and 3 is located in a byte within I/O space at an offset of 0xE from the adapter I/O base address. All bits are cleared with a power on reset. This *Write Only* register is structured as shown below.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
not used	not used	TXCS3	TXCS2	DTR3	DTR2	TX3	TX2
X	X	Port 3 0=output 1=input	Port 2 0=output 1=input	Port 3 0=inactive 1=active	Port 2 0=inactive 1=active	Port 3 0=disable 1=enable	Port 2 0=disable 1=enable

The TXCS3 and TXCS2 bits select the desired mode of the bi-directional transmit clock for ports 3 and 2 respectively. To use the transmit clock as an output, set this bit to 0. To use the transmit clock as input, program the internal registers of the Hitachi HD64570 to make transmit clock an input prior to setting this bit.

WARNING

If this bit is set to 1, and the Hitachi HD64570 is still outputting the transmit clock, two outputs will be tied together and damage to the HD64570 is possible.

X.21 Specific

Only one clock can be active on the X.21 connector. When using the DCE clock source, the X.21 Signal Element Timing input drives the HD64570 receive clock directly. The HD64570 RXS register should specify "Receive clock source is RXC line input." The HD64570 TXS register should specify "Transmit clock source is Receive clock."

When using the DTE clock source, the X.21 DTE Signal Element Timing output is also used as the transmit and receive clocks. The HD64570 RXS register should specify

"Receive clock source is Internal BRG output." The HD64570 TXS register should specify "Transmit clock source is Internal BRG output."

In both cases of X.21 clock sources, the SYNC/570 Transmit Clock and DTR Control register should specify the transmit clock as an output (TXCSn=0).

The Hitachi HD64570 does not directly support DTR. DTR is provided in this latch for compatibility with devices which require this signal.

Bits TX2 and TX3 of this register enable the transmitter of ports 2 and 3 respectively. When set to 0 (transmitter disabled), data may be transmitted from the Hitachi HD64570, but the data will not appear at the external connector.