

NOTES (block diagram only)  
 SPI = MOSI, MISO, SCLK, SSEL, ATTN  
 UART = TXD, RXD, CTS, RTS, CD, DTR (pin sleep)

- LEDs/ indicators
- RSSI (3 White LED Group)
- TX / RX / ASSOCIATE (Yellow White Blue LED group)
- ON\_nSLEEP (Blue LED)
- 5V Line (Red LED)
- FTDI Communication Enable (3 Yellow LED Group)
- Loopback (White LED)

TEST POINTS  
 2 x 0.1 Inch Header

COMMISSION BUTTON  
 (XLR\_DIO0/  
 AD0/  
 CommBtn)

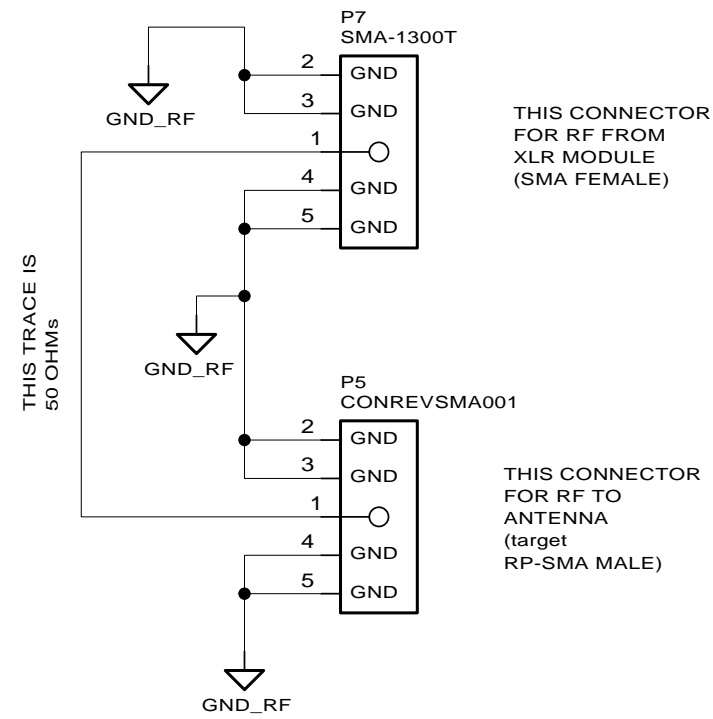
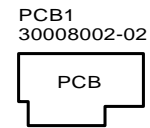
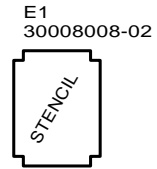
RESET CONTROL

RESET BUTTON

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

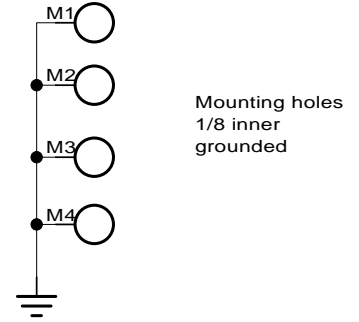
APPROVALS:	DATE:	TITLE
DESIGNED:	7/28/16	XLR Development Board -U
DRAWN:	xx/xx/xx	Block Diagram
CHECKED:	xx/xx/xx	
ENGINEER:	DLDatwyler PM/lett	PART NO.
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SHEET 1 of 13		

Mechanicals

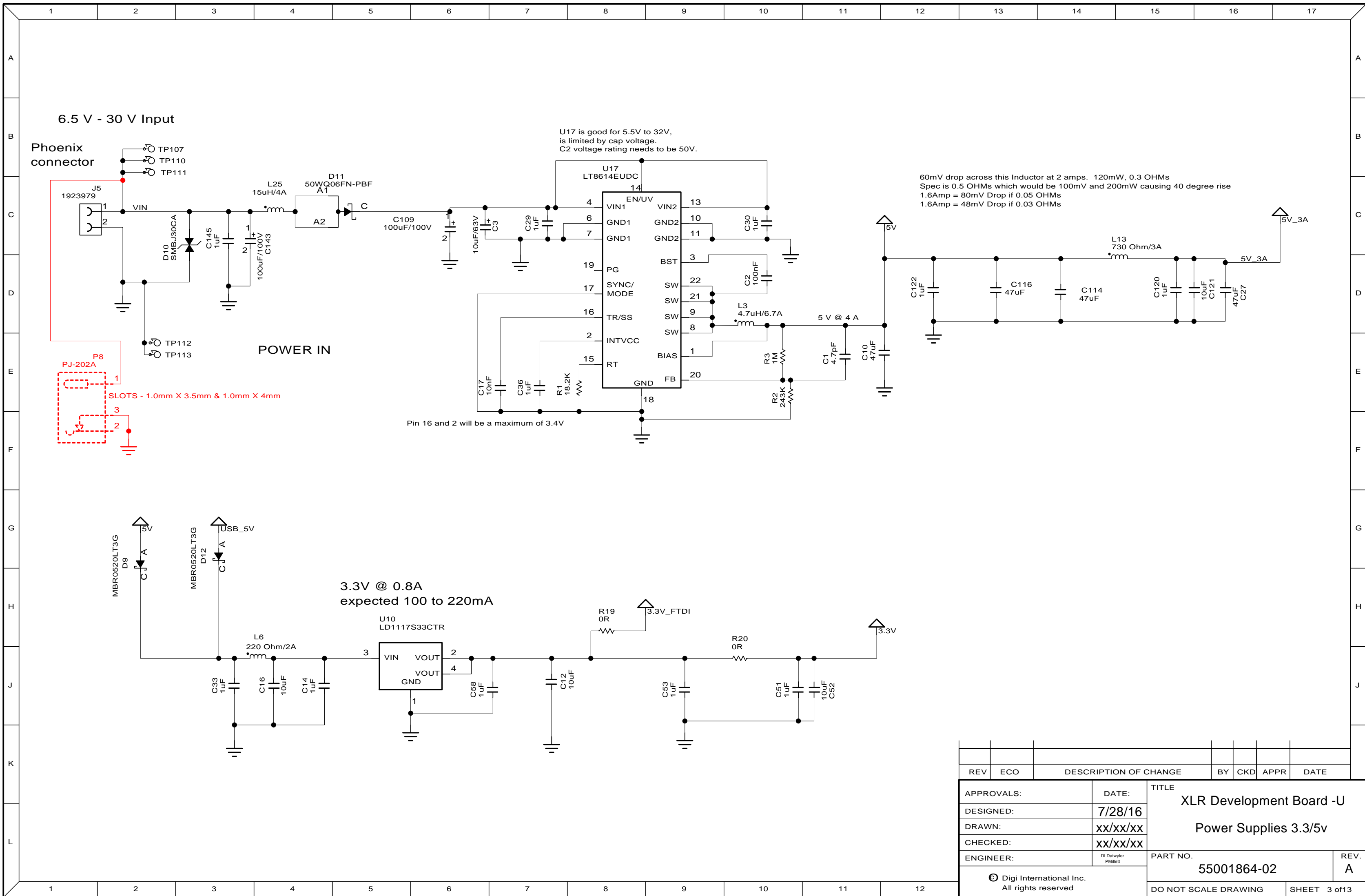


NO THERMAL RELIEF  
ON ANY LAYER  
VIAS IN EXPOSED METAL

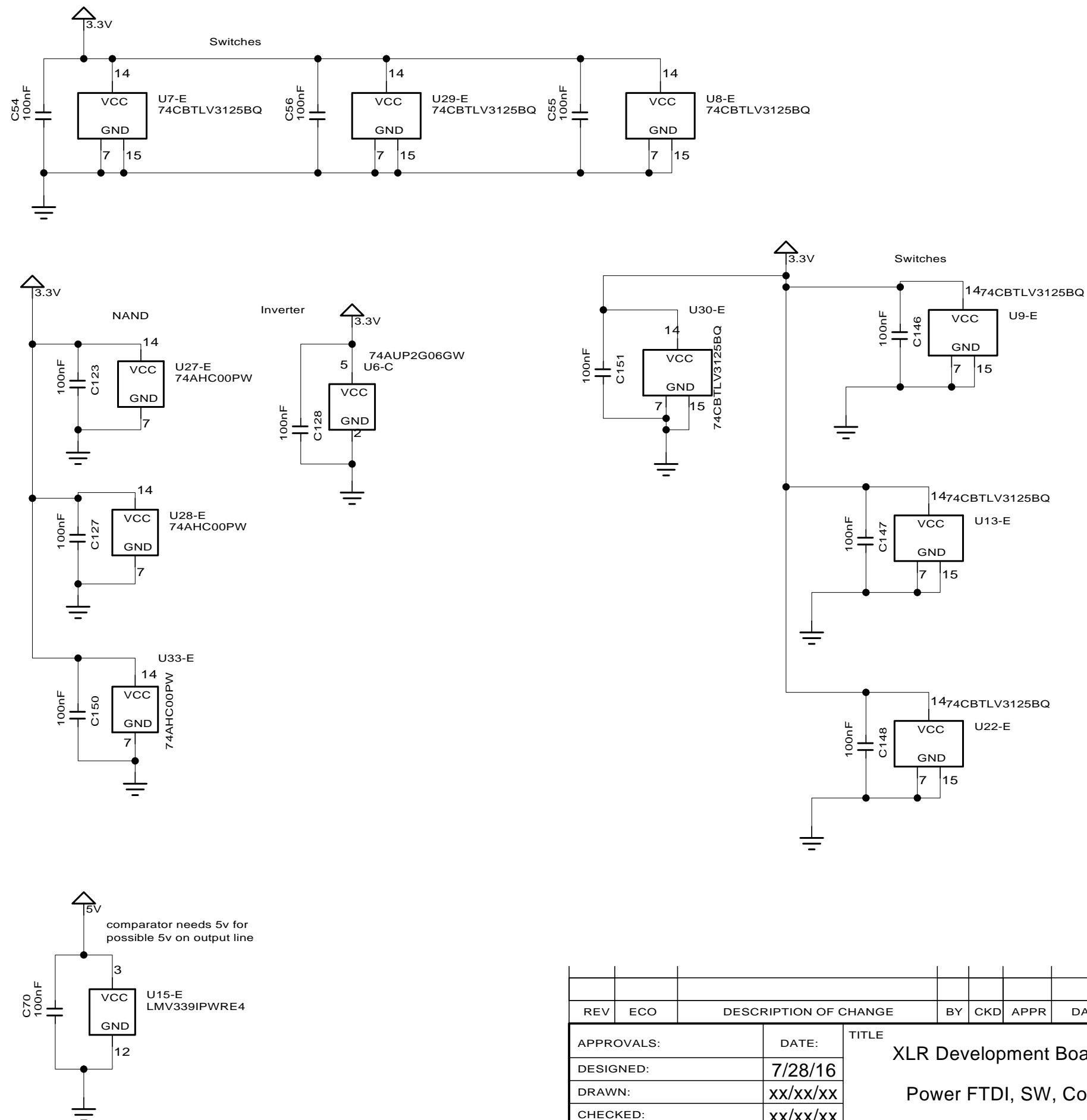
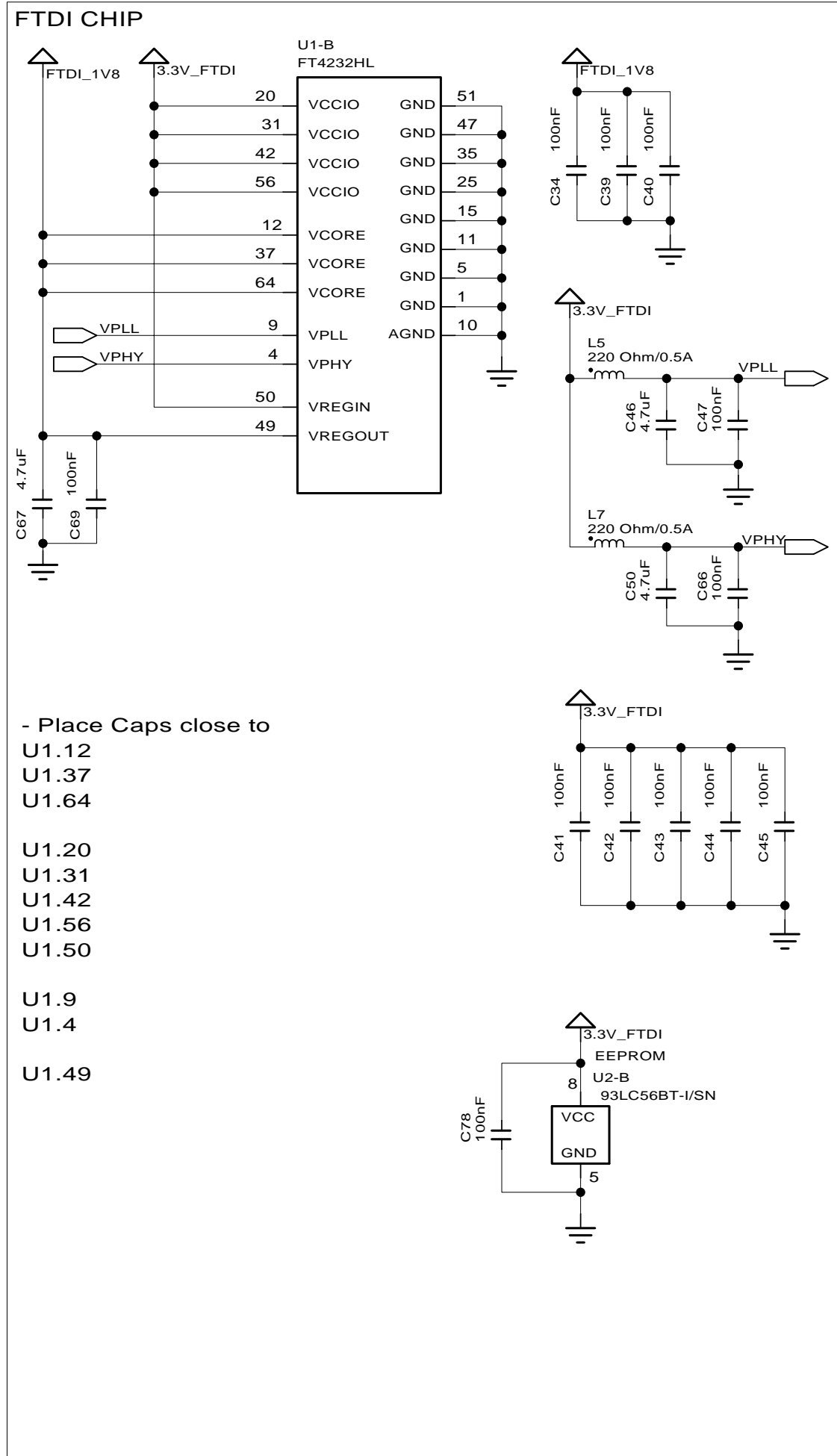
MULTIPLE VIAS THROUGH  
ALL GROUND LAYERS  
(USE A HEAVY "STITCH")



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		xx/xx/xx	Mechanicals			
CHECKED:		xx/xx/xx	PART NO.			
ENGINEER:		DLDatwyler PMillett	55001864-02		REV. A	
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					SHEET 2 of 13	



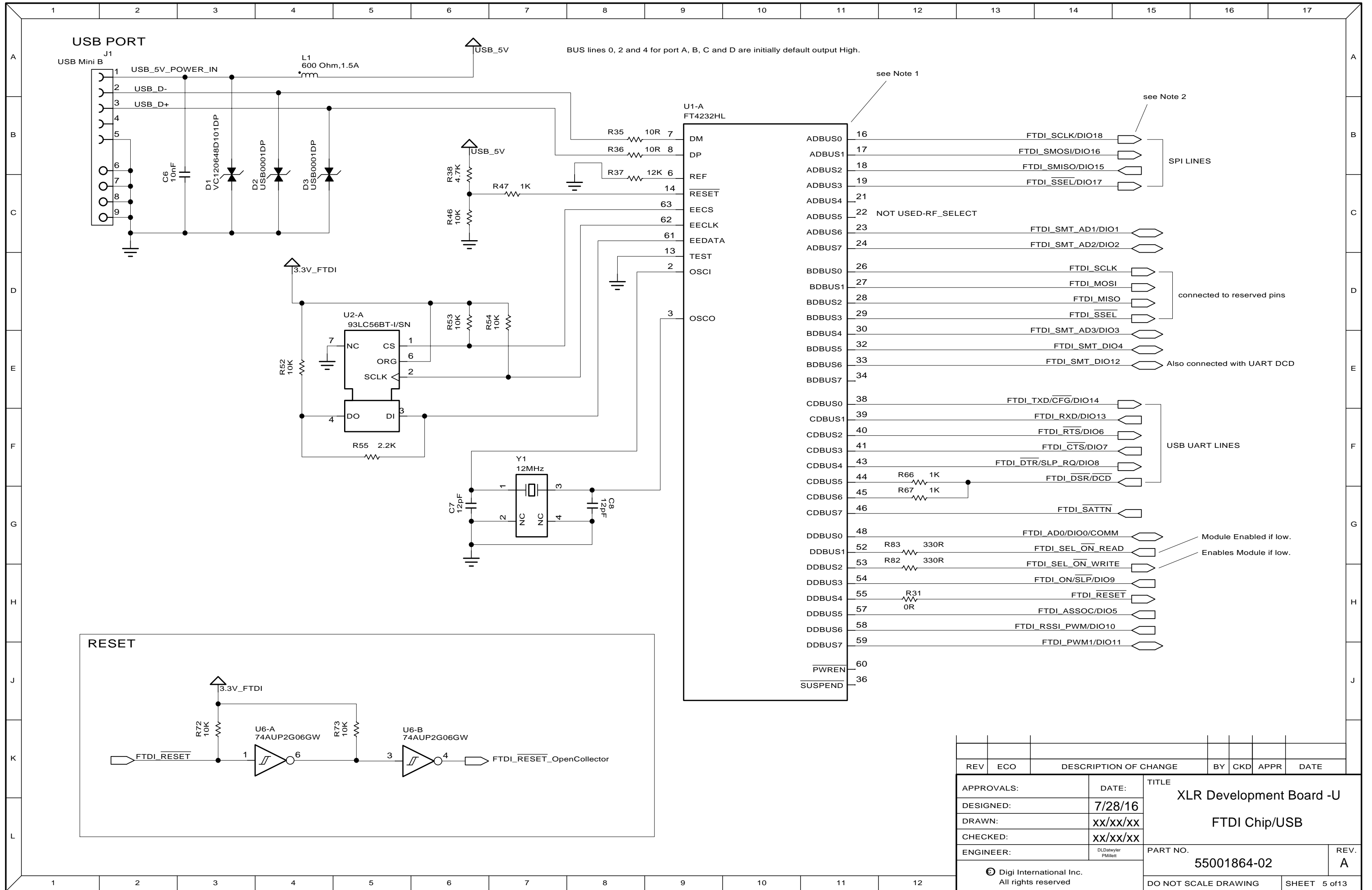
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		xx/xx/xx	Power Supplies 3.3/5v			
CHECKED:		xx/xx/xx	PART NO.			
ENGINEER:		DLDawyer PMIlett	55001864-02		REV. A	
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						SHEET 3 of 13



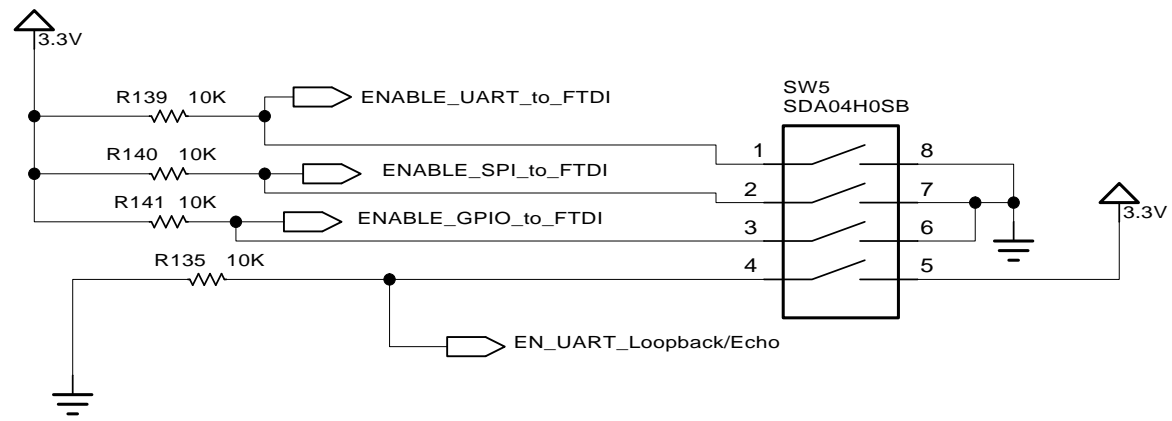
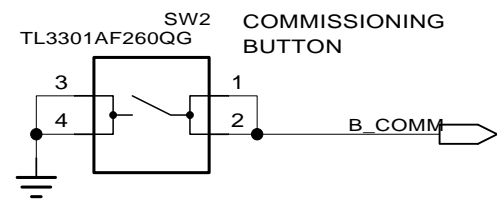
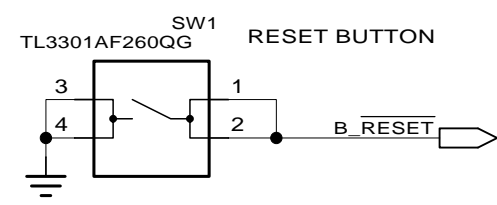
- Place Caps close to  
 U1.12  
 U1.37  
 U1.64  
  
 U1.20  
 U1.31  
 U1.42  
 U1.56  
 U1.50  
  
 U1.9  
 U1.4  
  
 U1.49

comparator needs 5v for possible 5v on output line

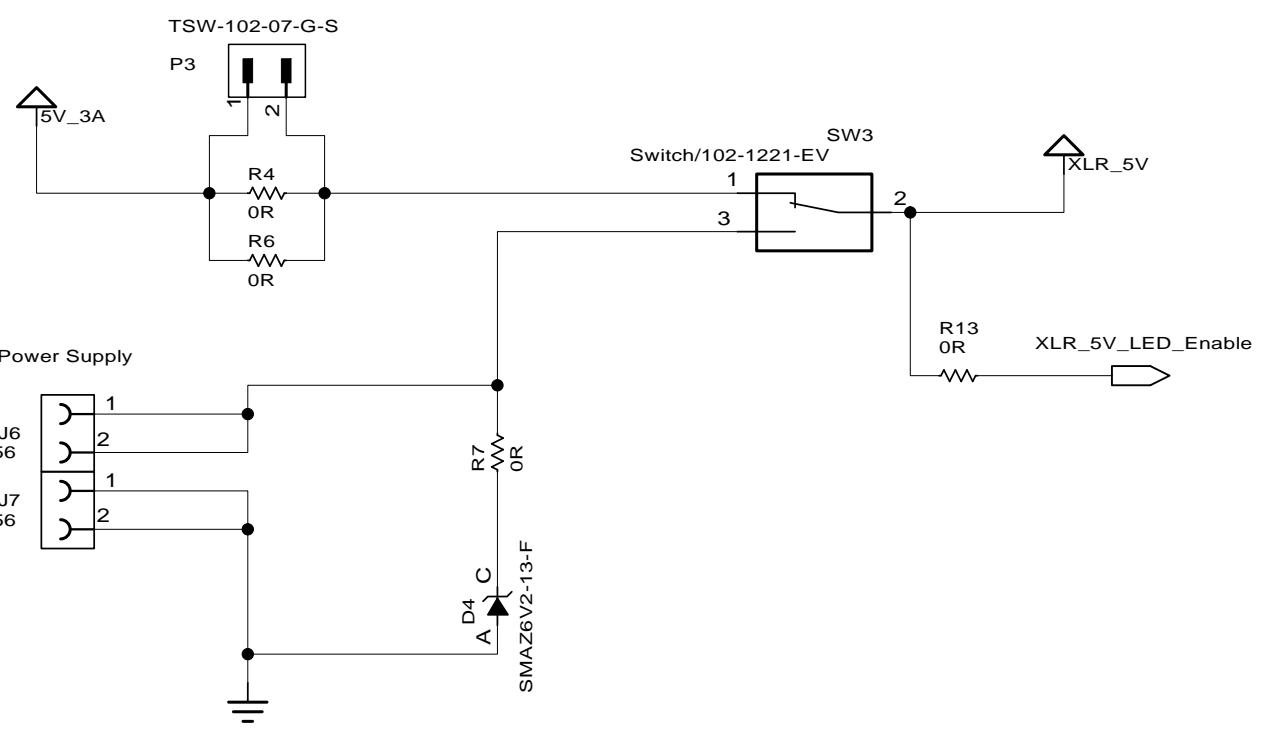
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		xx/xx/xx	Power FTDI, SW, Comp			
CHECKED:		xx/xx/xx				
ENGINEER:		DLDatwyler PMillett	PART NO.		REV.	
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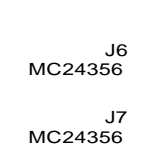
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		xx/xx/xx	FTDI Chip/USB			
CHECKED:		xx/xx/xx				
ENGINEER:		DL Dawleyler PK Millert	PART NO.		REV.	
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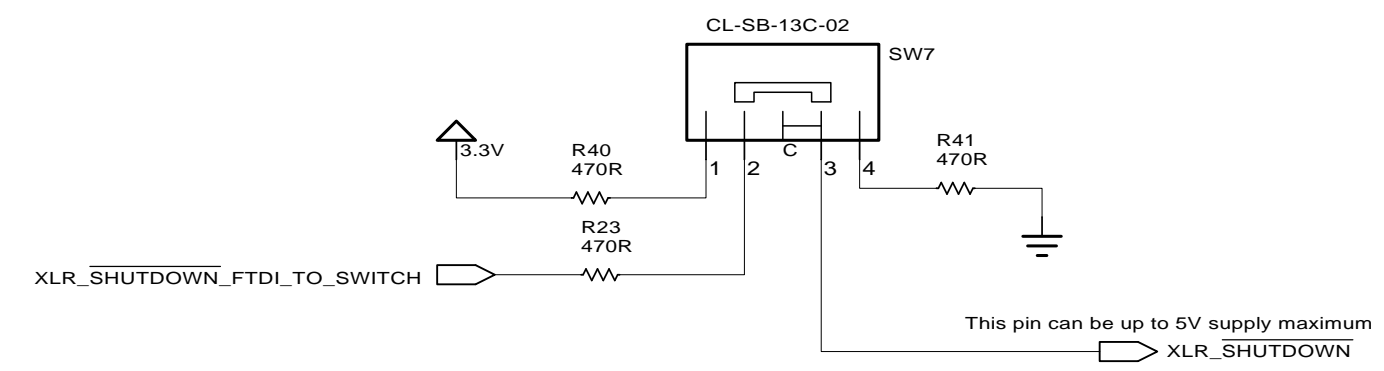
P3 can allow for in circuit current measurements if R4 and R6 are removed. However voltage drop may cause undesired operation when sudden current spikes occur during transmit.



5 V SENSE  
5 V FORCE  
GND FORCE  
GND SENSE



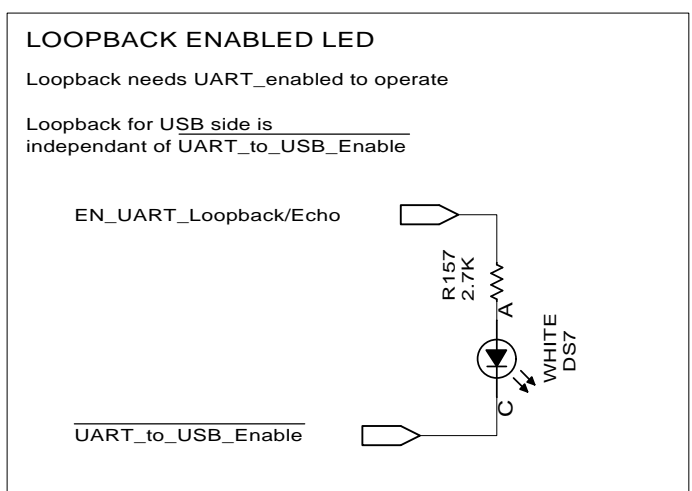
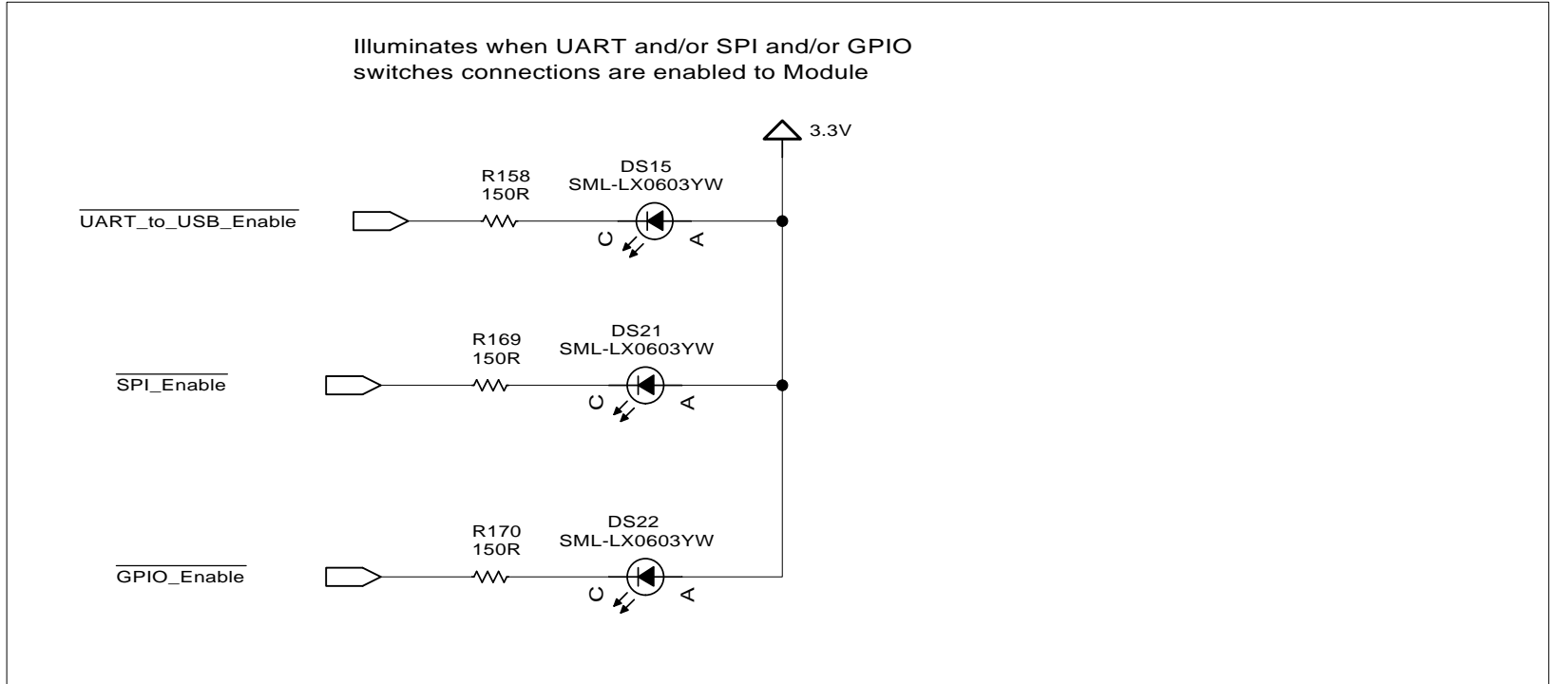
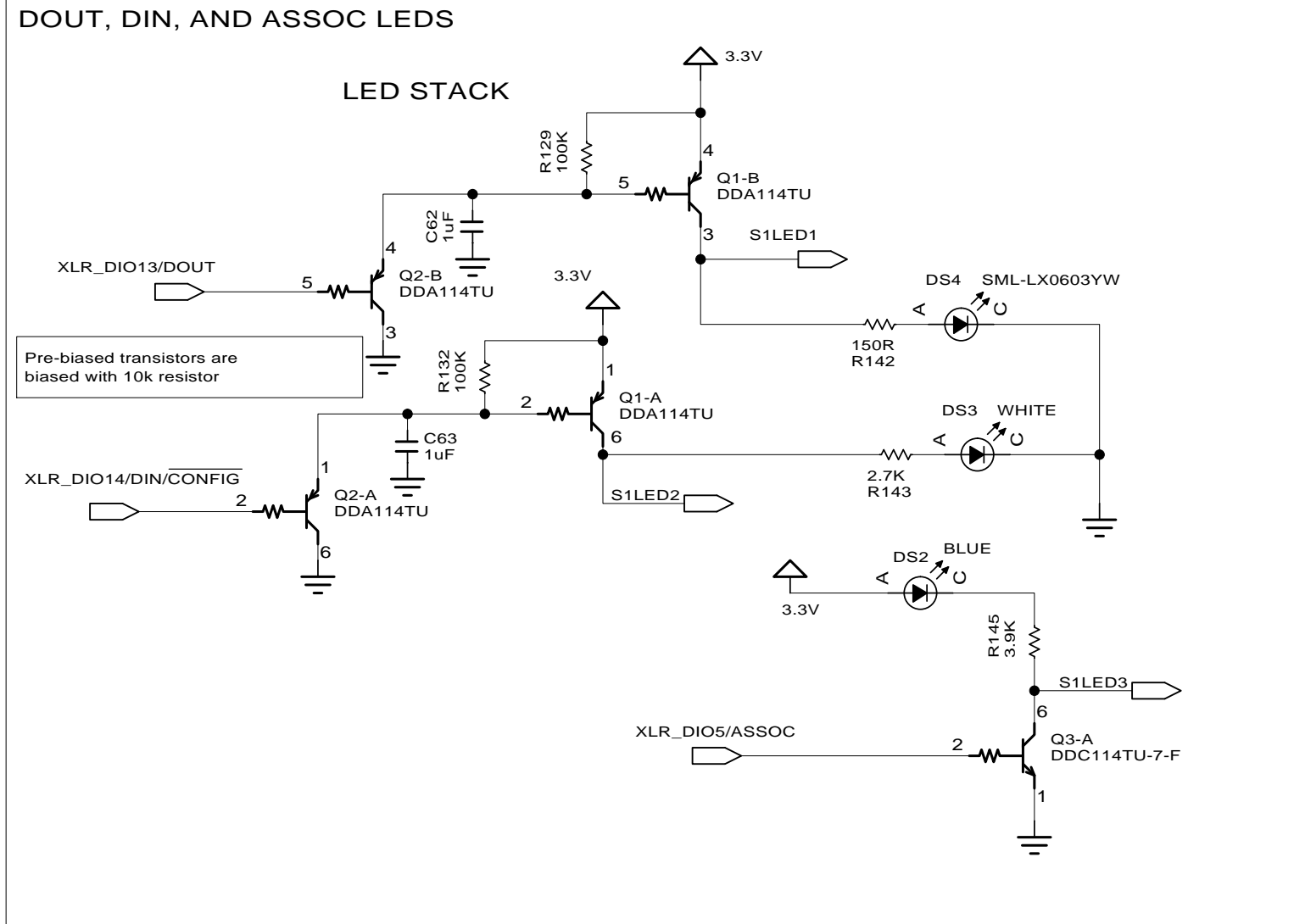
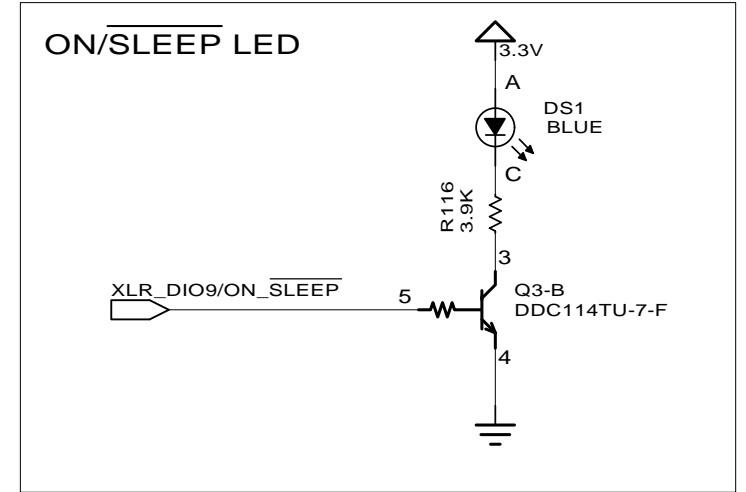
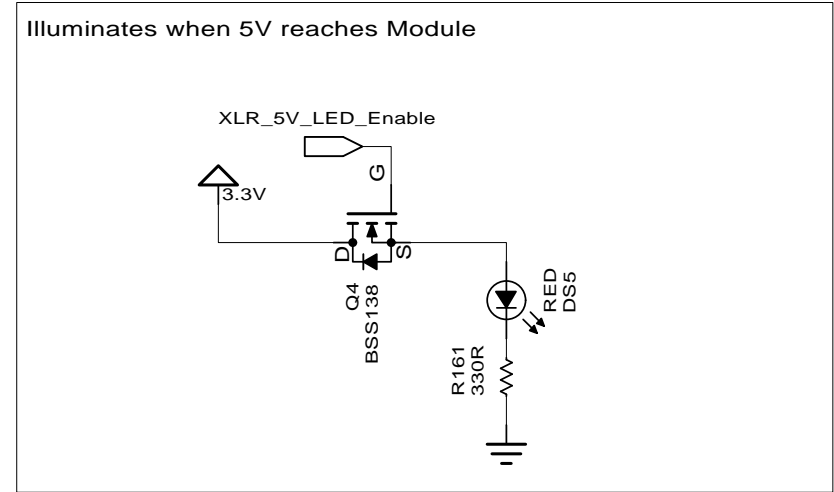
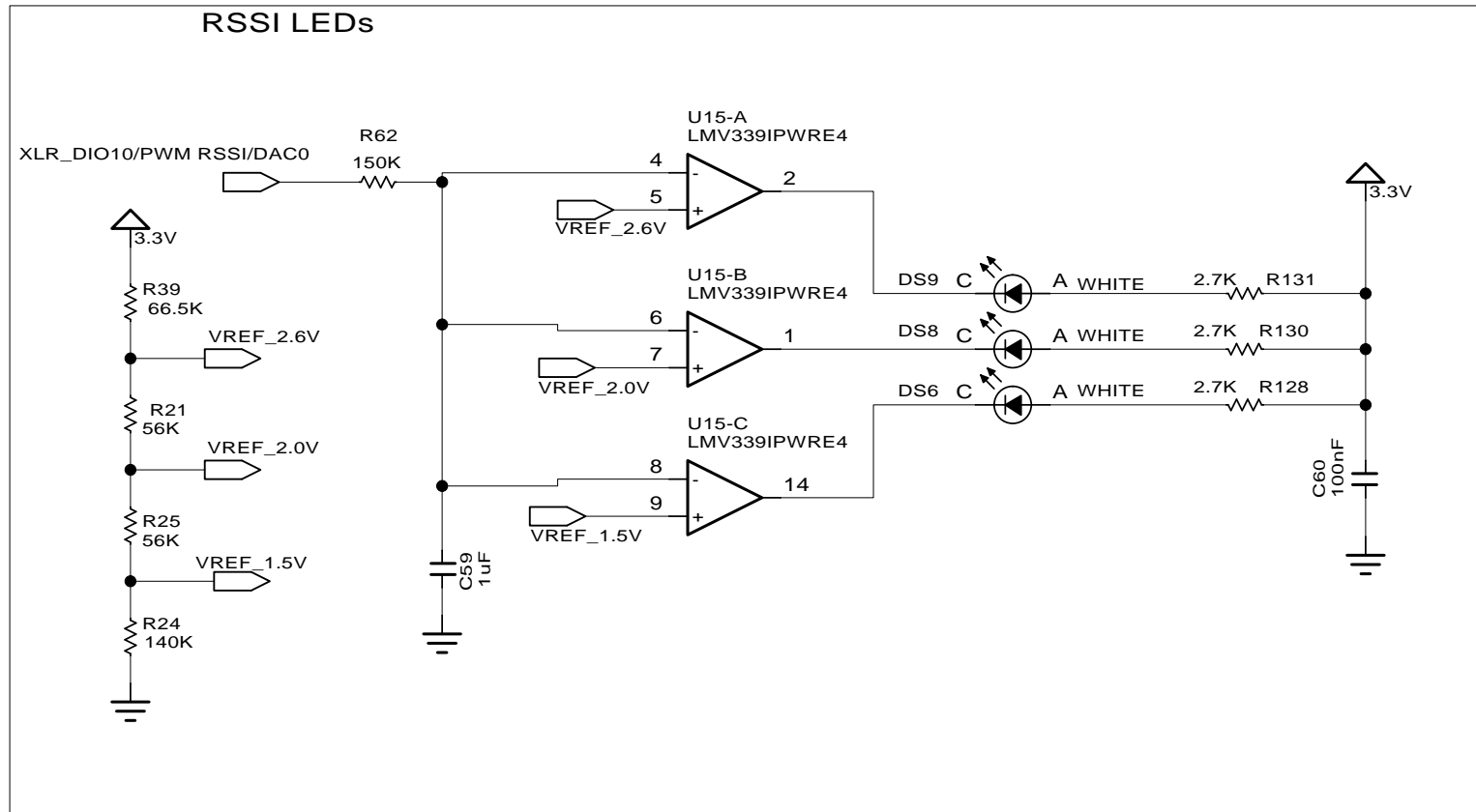
Switch Position	FTDI_SEL_ON_WRITE	XLR_Shutdown	Module 3.3V_OUT Enabled
High	X	High	Yes
Low	X	Low	No
Middle	Low	High	Yes
	High	Low	No



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

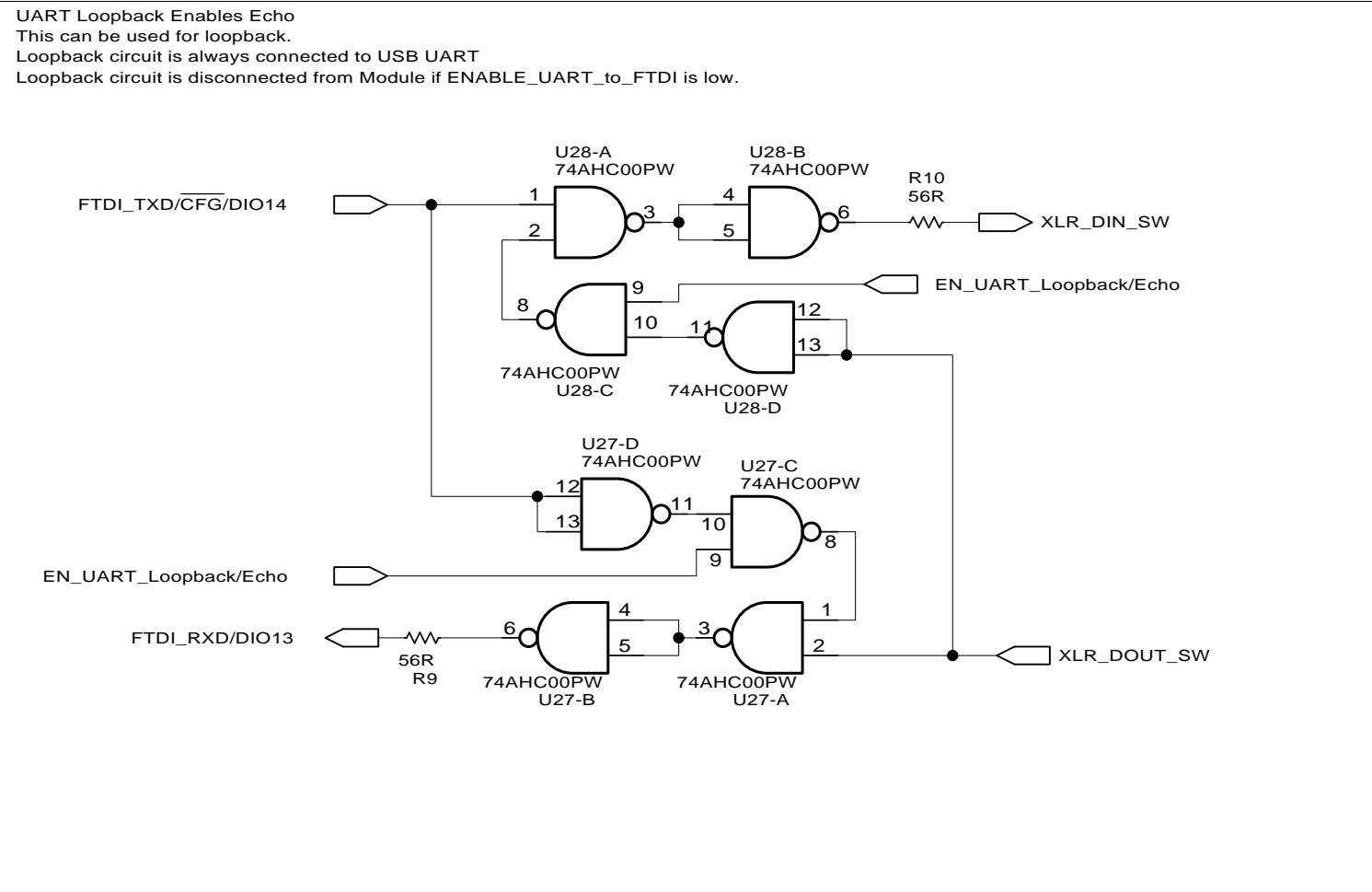
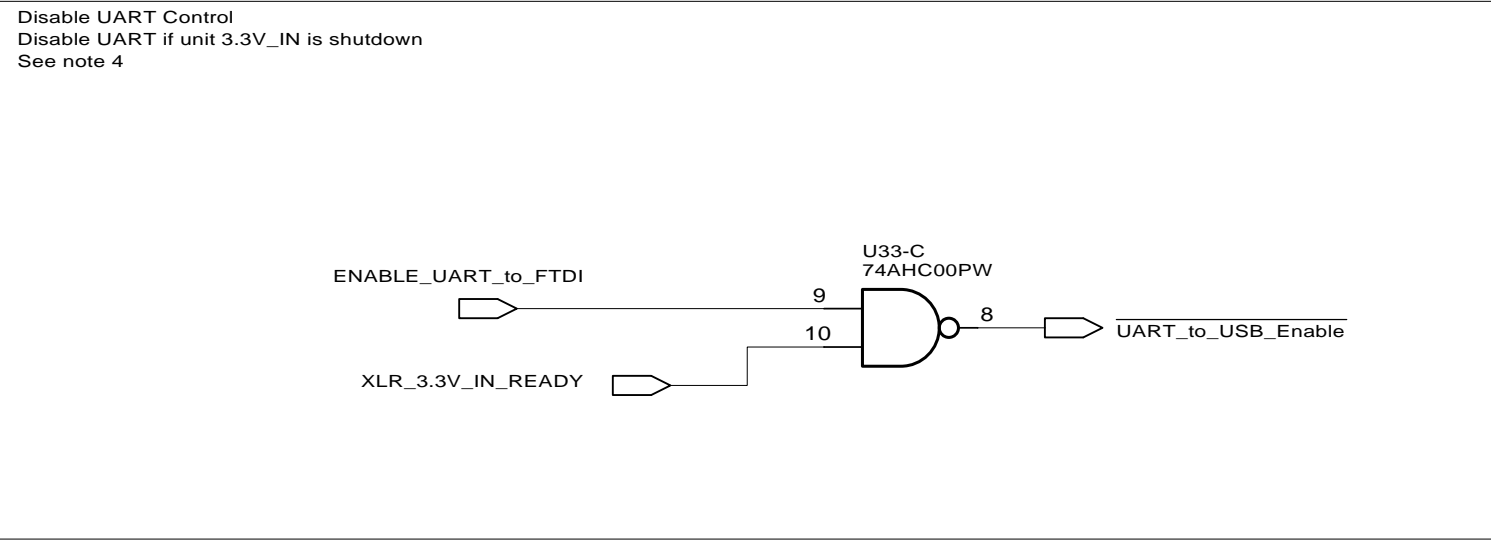
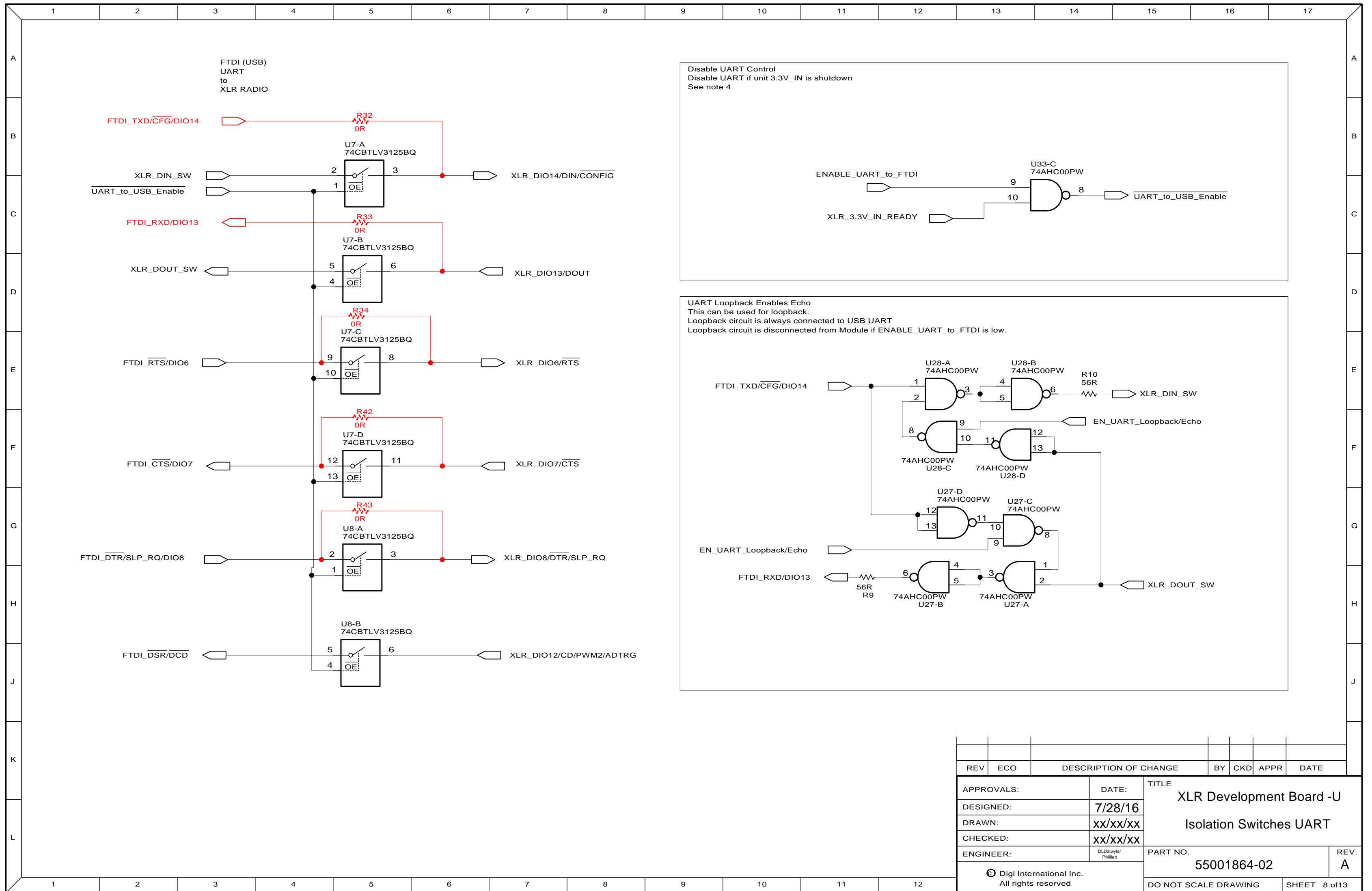
APPROVALS:	DATE:	TITLE
DESIGNED:	7/28/16	XLR Development Board -U
DRAWN:	XX/XX/XX	Buttons/Switches/Headers
CHECKED:	XX/XX/XX	
ENGINEER:	DL.Datwyler PMillett	PART NO.
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REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE

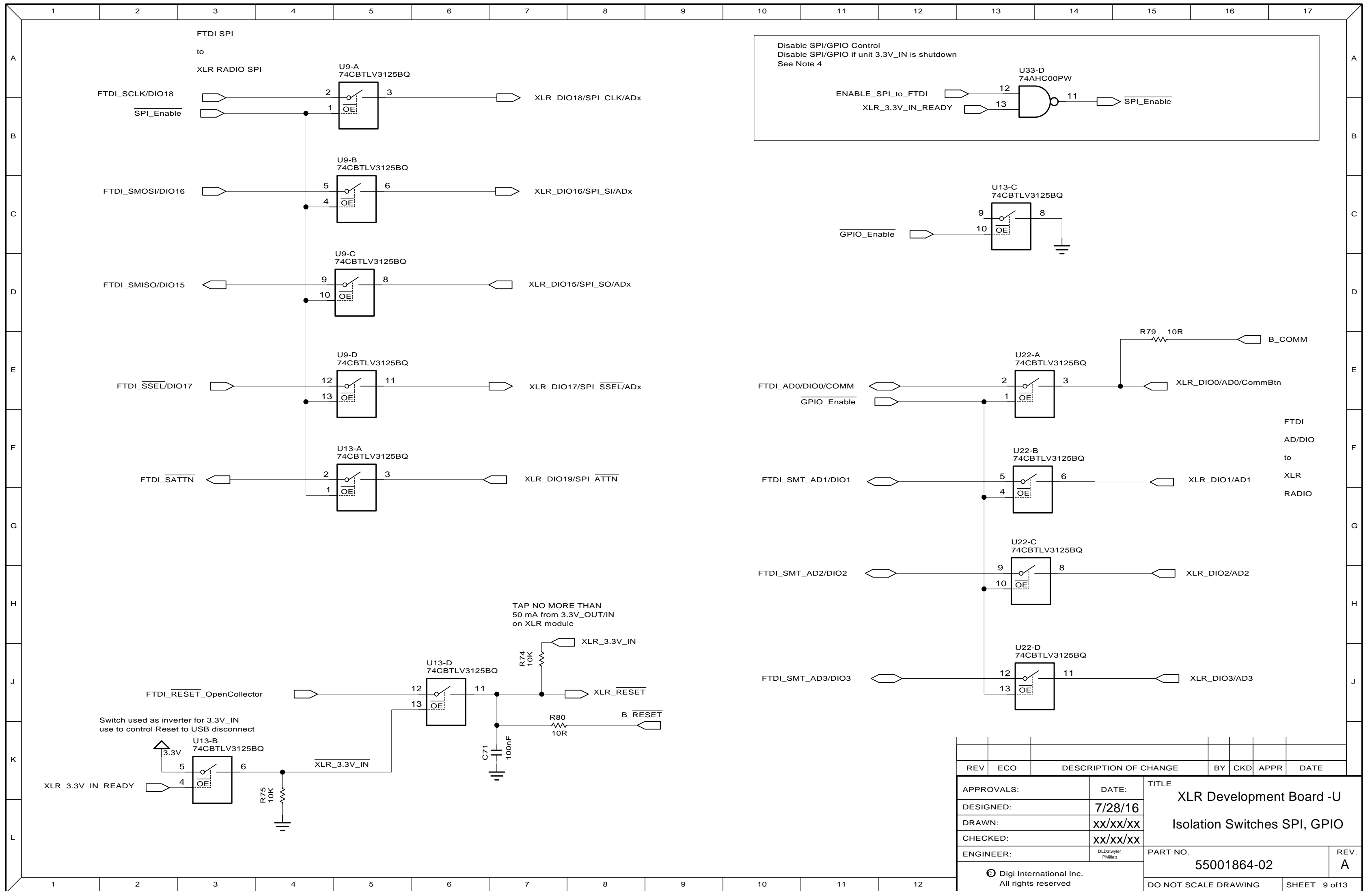
  

APPROVALS:	DATE:	TITLE
DESIGNED:	7/28/16	XLR Development Board -U
DRAWN:	XX/XX/XX	LEDs
CHECKED:	XX/XX/XX	
ENGINEER:	DLDatwyler PMillett	PART NO.
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DO NOT SCALE DRAWING		REV. A
SHEET 7 of 13		

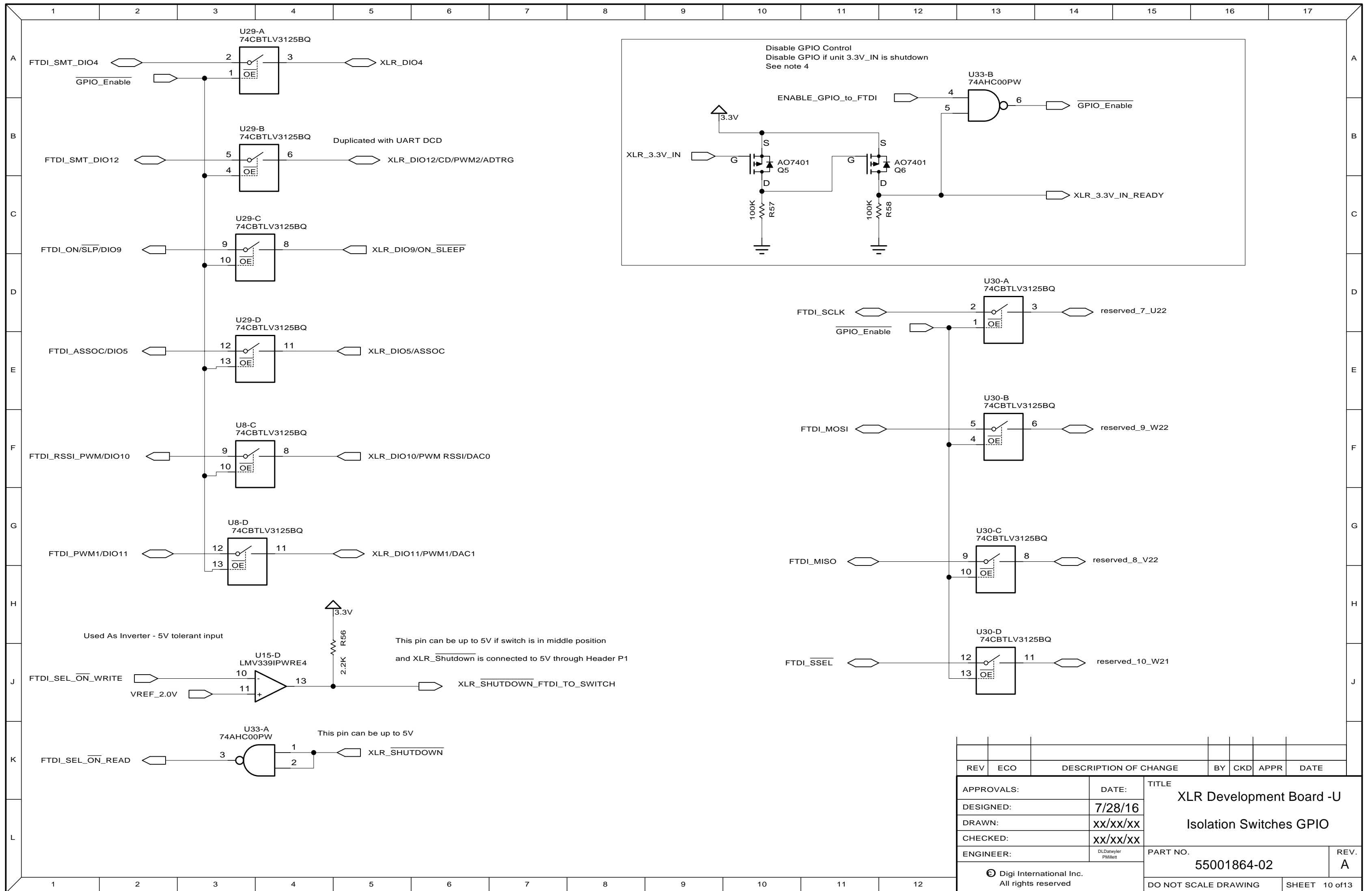


REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE	
APPROVALS:		DATE:	TITLE				
DESIGNED:		7/28/16	XLR Development Board -U				
DRAWN:		xx/xx/xx	Isolation Switches UART				
CHECKED:		xx/xx/xx	PART NO.				
ENGINEER:		DLDatwyler PMillett	55001864-02		REV. A		
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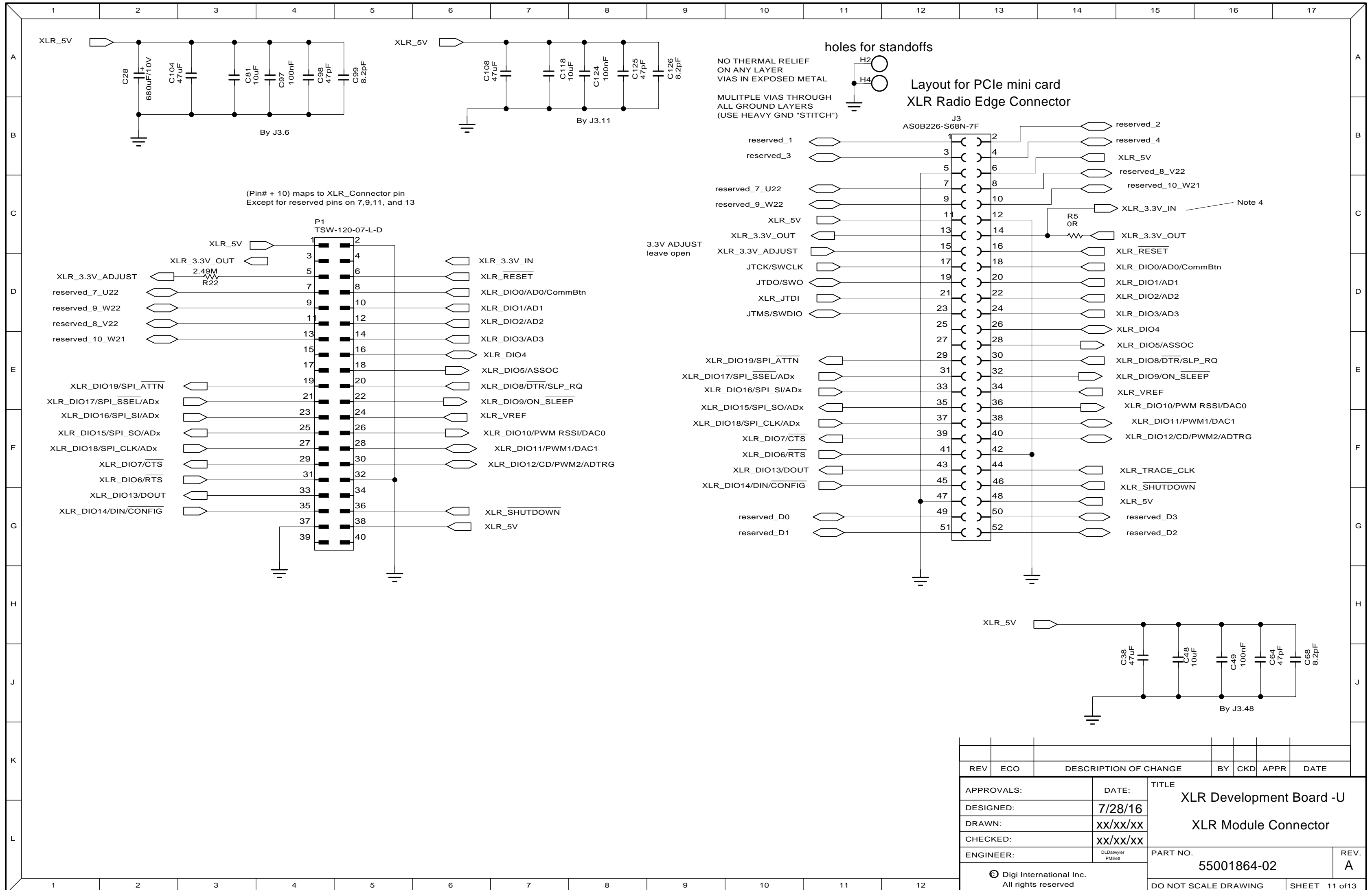




REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		xx/xx/xx	Isolation Switches SPI, GPIO			
CHECKED:		xx/xx/xx	PART NO.			
ENGINEER:		DL.Datwyler PM/ilett	55001864-02		REV. A	
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						SHEET 9 of 13



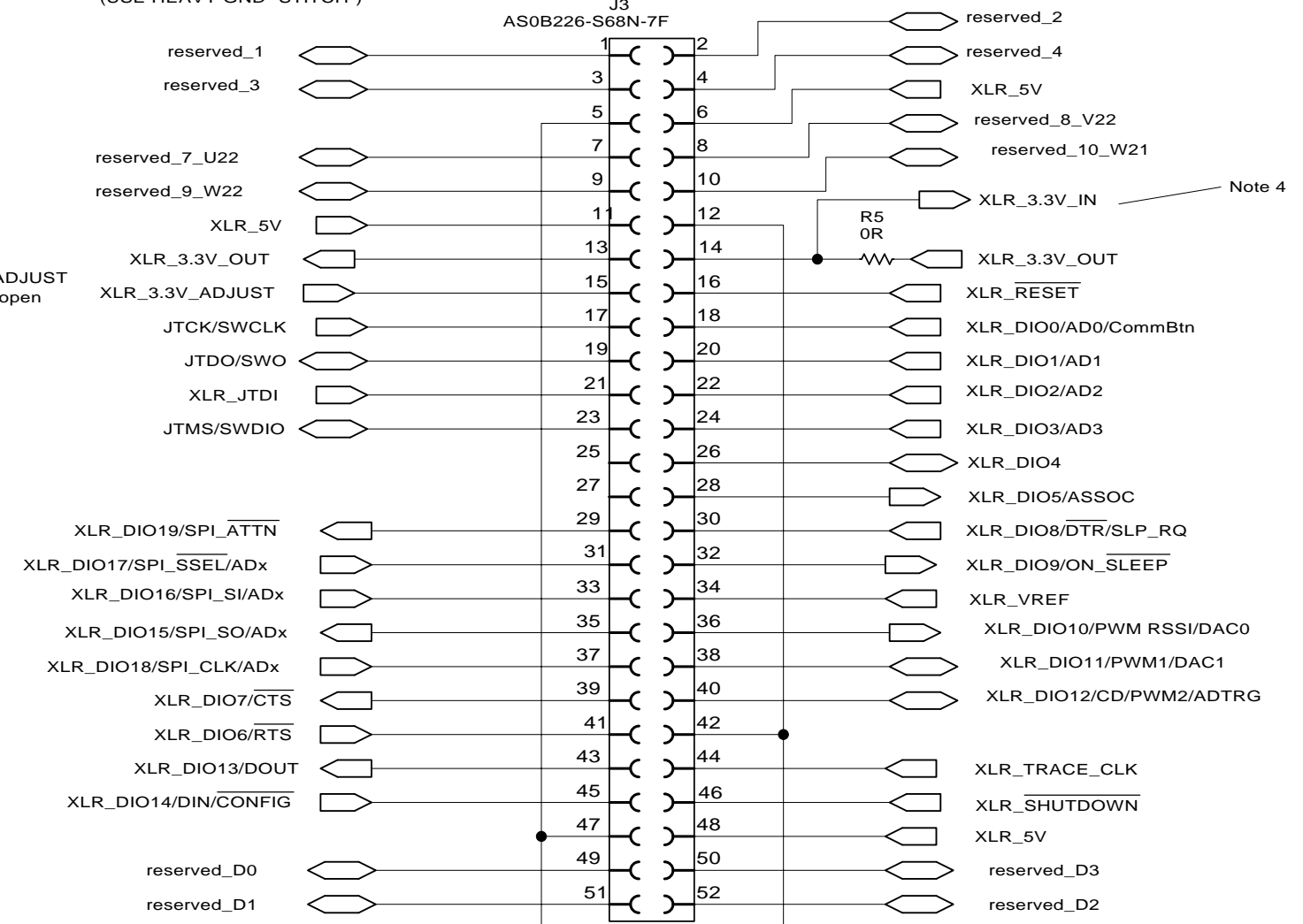
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		XX/XX/XX	Isolation Switches GPIO			
CHECKED:		XX/XX/XX				
ENGINEER:		DLDatwyler PMillet	PART NO.		REV.	
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(Pin# + 10) maps to XLR\_Connector pin  
Except for reserved pins on 7,9,11, and 13

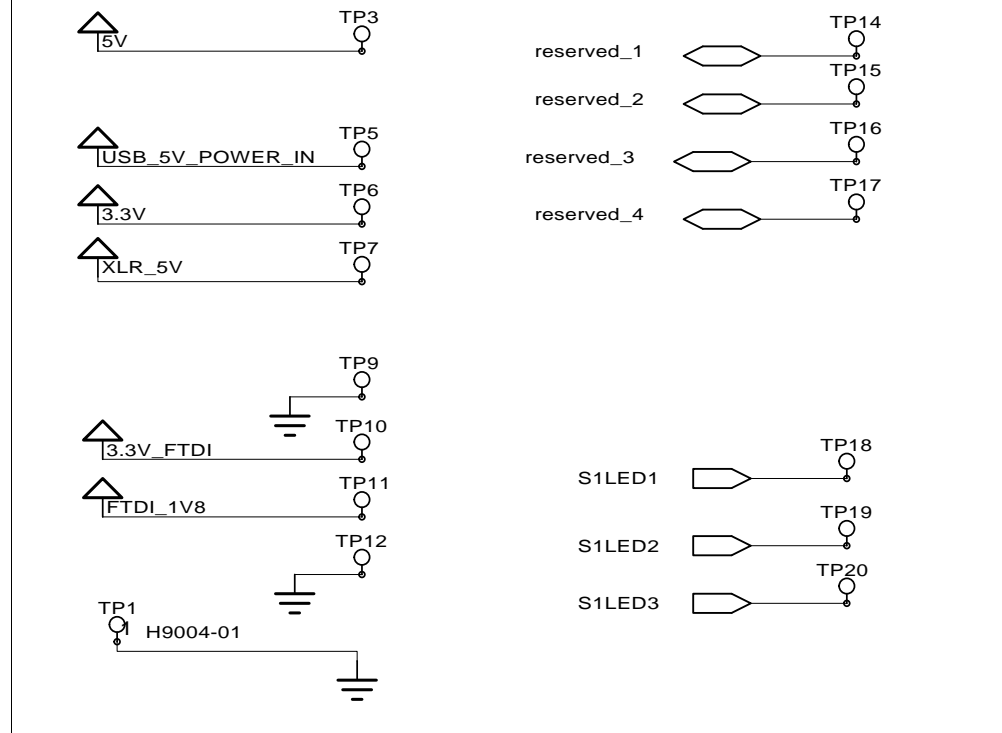
holes for standoffs  
NO THERMAL RELIEF ON ANY LAYER  
VIAS IN EXPOSED METAL  
MULTIPLE VIAS THROUGH ALL GROUND LAYERS (USE HEAVY GND "STITCH")

Layout for PCIe mini card  
XLR Radio Edge Connector

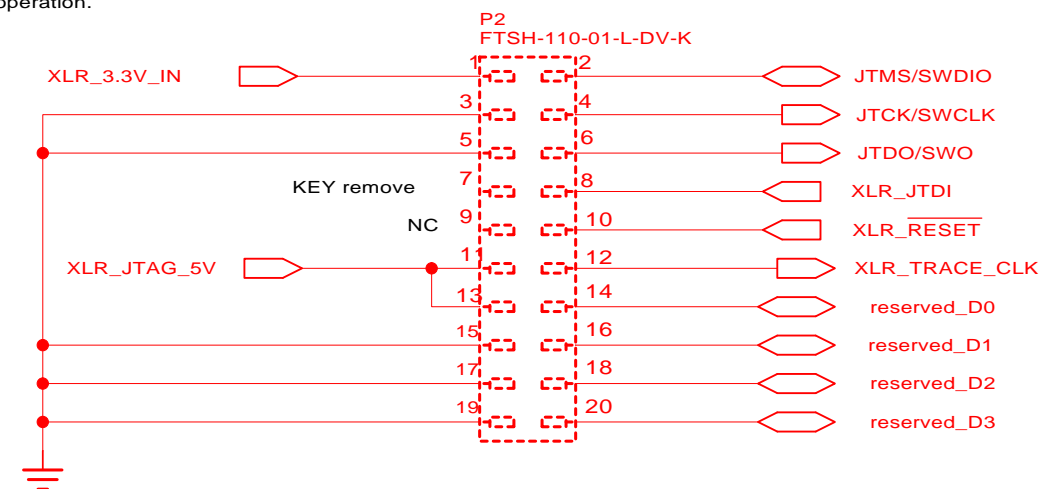


REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		XX/XX/XX	XLR Module Connector			
CHECKED:		XX/XX/XX	PART NO.			
ENGINEER:		DLDehwyler PMMillett	55001864-02		REV. A	
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### TEST POINTS



The JTAG/SWD pins are referenced to 3.3 V from the XLR. This must be here for proper JTAG/SWD operation.



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:		7/28/16	XLR Development Board -U			
DRAWN:		XX/XX/XX	Test Points			
CHECKED:		XX/XX/XX	PART NO.			
ENGINEER:		D. Datwyler PM/lett	55001864-02		REV. A	
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						SHEET 12 of 13

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A																		A
B																		B
C																		C
D																		D
E																		E
F																		F
G																		G
H																		H
J																		J
K																		K
L																		L
	1	2	3	4	5	6	7	8	9	10	11	12						

**Notes**

- The FT4232H chip has 4 separate I/O ports. Each of these ports can be set to different modes at any time. Only one mode can be set on a port at a time. All of the ports can be set to serial, asynchronous bit-bang, or synchronous bit-bang. Only ports A and B can be set to MPSSE mode, which includes SPI, I2C, and JTAG modes. The default state for all of the ports will be UART for first time plug in. This cannot be changed until after programming EEPROM.
- The FT4232H chip supports two modes for the SPI clock. The first mode supports speeds from 92 Hz to 6 MHz and follows the equation below (CD is the clock divisor and must be an integer:  

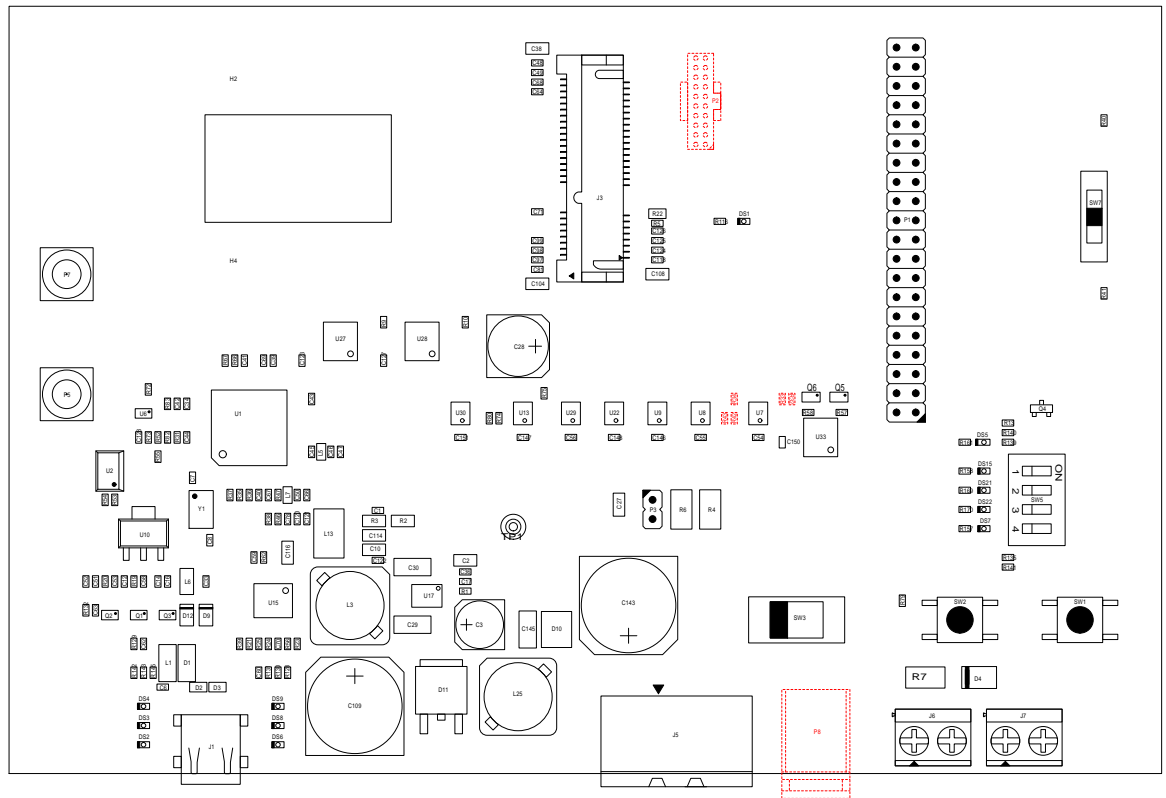
$$f = 12\text{MHz} / (2 * (1 + \text{CD}))$$

The other mode can handle speeds between 460 Hz and 30 MHz and follows the equation below:

$$f = 60\text{ MHz} / (2 * (1 + \text{CD}))$$

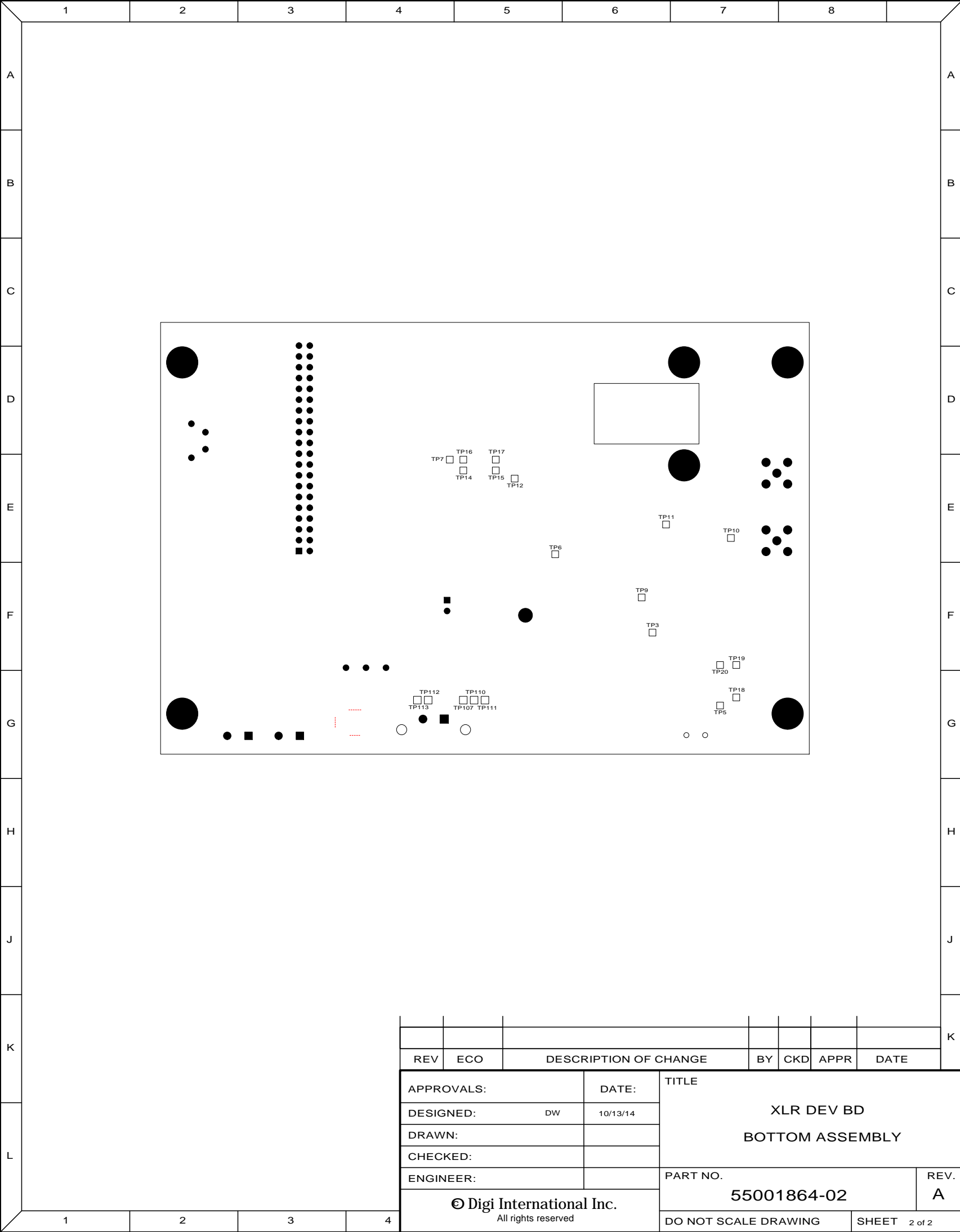
The MOSI and MISO lines are synchronous with the SPI clock. All of the other GPIO pins are not.
- Since the FTDI chip is powered by 3.3V. The XLR 3.3V\_IN must be limited between 3 to 3.5V when connections are enabled. To test the XLR at a lower voltage, all FTDI connections must be disabled, with XLR\_nShutdown low. An external supply can be inserted to 3.3V\_IN as long as it complies with Manual requirements and signal integrity is observed.
- If 3.3V\_IN is low all DIO pins must be tri-state or low. Pullups are not allowed in this state.
- Signal integrity should always be observed on all pins. ONLY 5V pins and XLR\_SHUTDOWN can receive volages higher than 3.3V\_IN. All digital lines are based off of 3.3V\_IN.
- 5V supply is still needed for XLR module to receive or transmit regardless of what voltage is on 3.3V\_IN

REV	ECO	DESCRIPTION OF CHANGE										BY	CKD	APPR	DATE					
APPROVALS:		DATE:		TITLE																
DESIGNED:		7/28/16		XLR Development Board -U																
DRAWN:		XX/XX/XX		Notes																
CHECKED:		XX/XX/XX																		
ENGINEER:		DLDatwyler PMillett		PART NO.										REV.						
				55001864-02										A						
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**Note:**  
All testpoints on bottom side - no solder allowed on pads.

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE			
DESIGNED:			XLR DEV BD TOP ASSEMBLY			
DRAWN:						
CHECKED:						
ENGINEER:			PART NO.			REV.
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REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS:		DATE:	TITLE <b>XLR DEV BD</b> <b>BOTTOM ASSEMBLY</b>			
DESIGNED: DW		10/13/14				
DRAWN:						
CHECKED:						
ENGINEER:						
<b>© Digi International Inc.</b> All rights reserved			PART NO.		REV.	
			55001864-02		A	
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